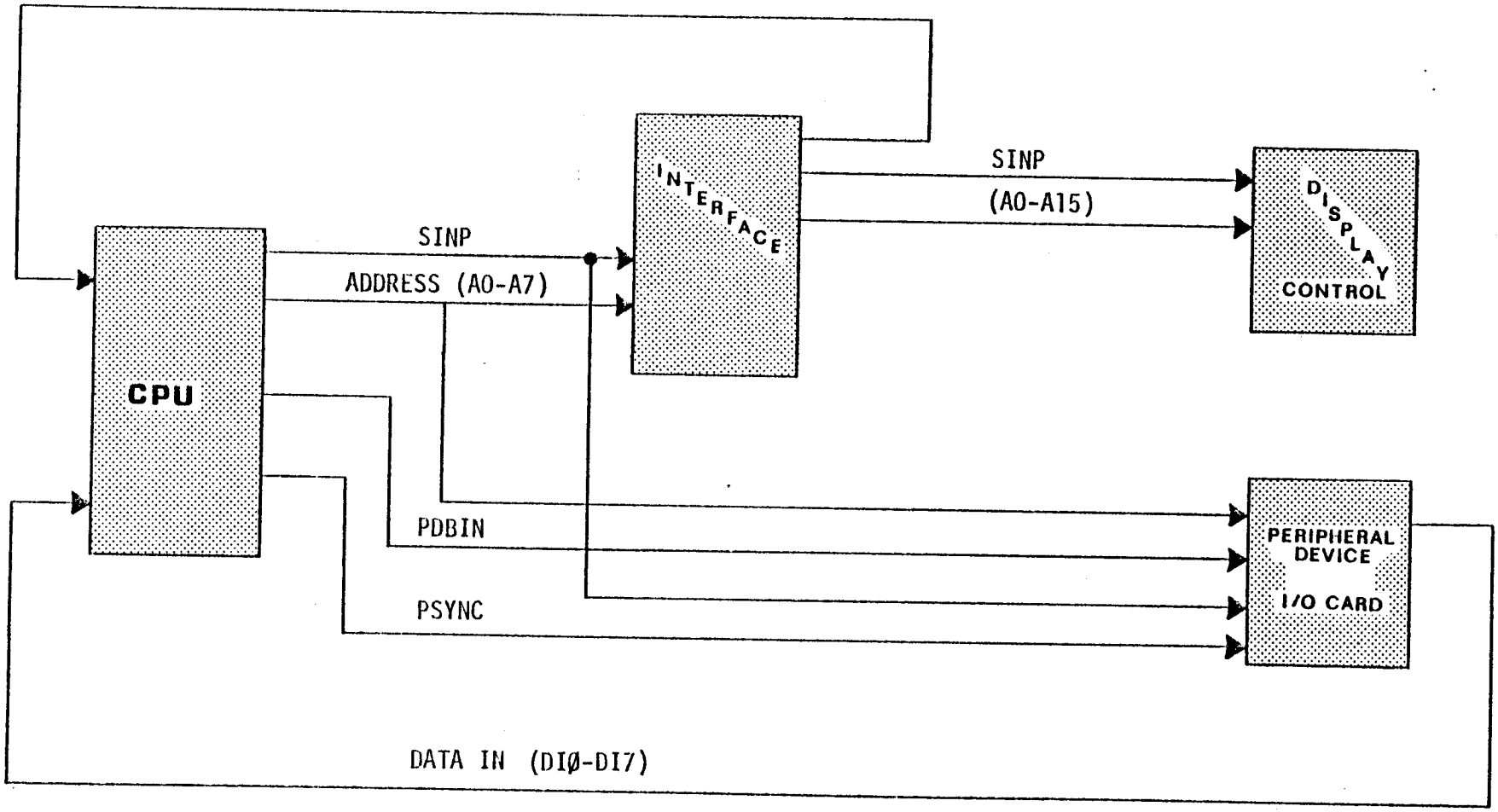

Figure 3-6. Input Read Cycle Block Diagram

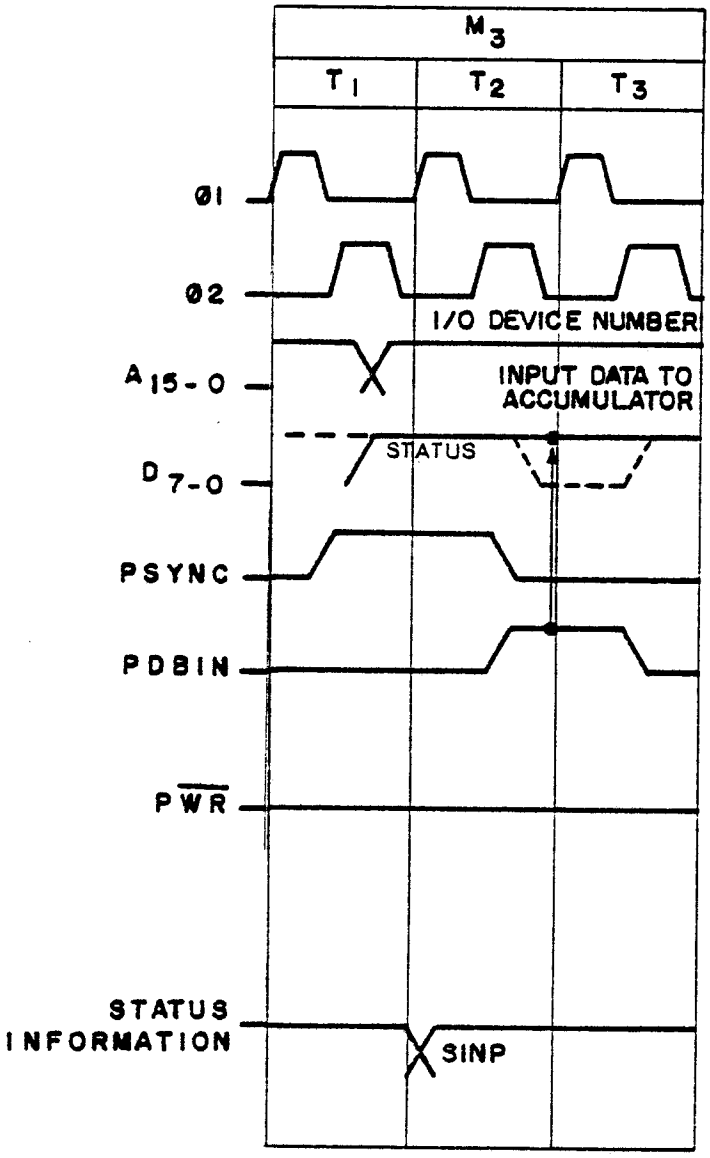

Figure 3-7. Input Read Cycle Timing.

presented to the Display/Control card. The AØ through A15 signals present on the Display/Control card (Figure 3-16, sheet 3, zone A9-A4) light the appropriate AØ through A15 LEDs, indicating the address of the external device. (Recall that when addressing an I/O device, the address is repeated on the upper eight and lower eight address LEDs.) The DØ through D7 data is applied to K (Figure 3-14, zone B5) on the CPU through the bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7), conditioning F to generate a signal during T2.

At the beginning of T2, a $\overline{STSTB}$ (zone B7) is generated LOW from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5), allowing the status data DØ through D7 to be stored into K. The status data present at the output of K conditions the I/O card to send data to the CPU by enabling the SINP signal.

A SINP output from K is presented HIGH on pin 46 of the bus (zone A4) through non-inverting bus driver R. The SINP signal is applied through inverter V on the Interface Card (Figure 3-15, sheet 2, zone B5) and presented to the Display/Control card as $\overline{SINP}$. The $\overline{SINP}$ signal present on the Display/Control card lights the INP LED (Figure 3-16, sheet 3, zone C3) on the front panel of the 8800b, indicating data is being received from an external device. The SINP output from the CPU is applied to the external device I/O card in order to initiate a data transfer to the CPU during T3.

At the beginning of T3, the external device data is transferred to M on the CPU via the bus. The external device data in (DIØ through DI7) is applied to the CPU card (Figure 3-14, zone B1) from the bus. The data is presented to the 8080 (M) through bi-directional gates D and E (zone C7), inverter bus drivers L and J (zone B4), and inverters Y and S (zone B3) by the PDBIN signal.

At the latter portion of T2 and the beginning of T3, a DBIN output (zone C8) HIGH is generated by M. The DBIN output is applied to the $\overline{DIEN}$ inputs (zone C7) of D and E, pin 4 of NAND gate C (zone B4) and the bus pin 78 (zone D1) as PDBIN. This

signal enables pin 6 of NAND gate C LOW (DIG 1 is HIGH when the front panel is not used), allowing the data input from the I/O card (DIØ-DI7) to be enabled through inverting bus drivers L and J (zone B4) and applied through bi-directional gates D and E to M (zone C7). The data at the external device is presented on the bus by the occurrence of PDBIN. After the external device data is stored in the CPU, the P counter is incremented, thus ending the Input Read Cycle operation.

3-21. CPU TO MEMORY DATA TRANSFER

A CPU to Memory data transfer is accomplished whenever an instruction is encountered to perform this operation. For example, a store accumulator STA (062_8) instruction requires the accumulator in the CPU to transfer its contents to memory. The STA instruction is fetched during M1 and its storage location determined in memory read cycles M2 and M3. The accumulator data is transferred to memory by a Memory Write Cycle operation (M4).

3-22. MEMORY WRITE CYCLE BASIC OPERATION (Figure 3-8)

The Memory Write Cycle operation will allow the CPU to transfer data to the memory. Several signals are generated by the CPU in order to transfer data to the memory.

The $\overline{\text{SWO}}$ output from the CPU is applied to the Display/Control through the Interface to light the WO (write out) LED on the 8800b front panel. The ADDRESS ($XXX\ XXX_8$), consisting of fifteen individual outputs (AØ-A15) from the CPU, is presented to the Display/Control and memory. The AØ through A15 signals light the appropriate address LEDs on the Display/Control. The ADDRESS and PSYNC signals present at the memory from the CPU can also initiate decoding of the memory address. With the memory conditioned, eight DATA OUT lines (DOØ-DO7) transfer the CPU data to the memory for storage. The $\overline{\text{PWR}}$ and $\overline{\text{SOUT}}$ outputs from the CPU are applied to the Interface to produce a MWRITE signal which allows the memory to store the data.

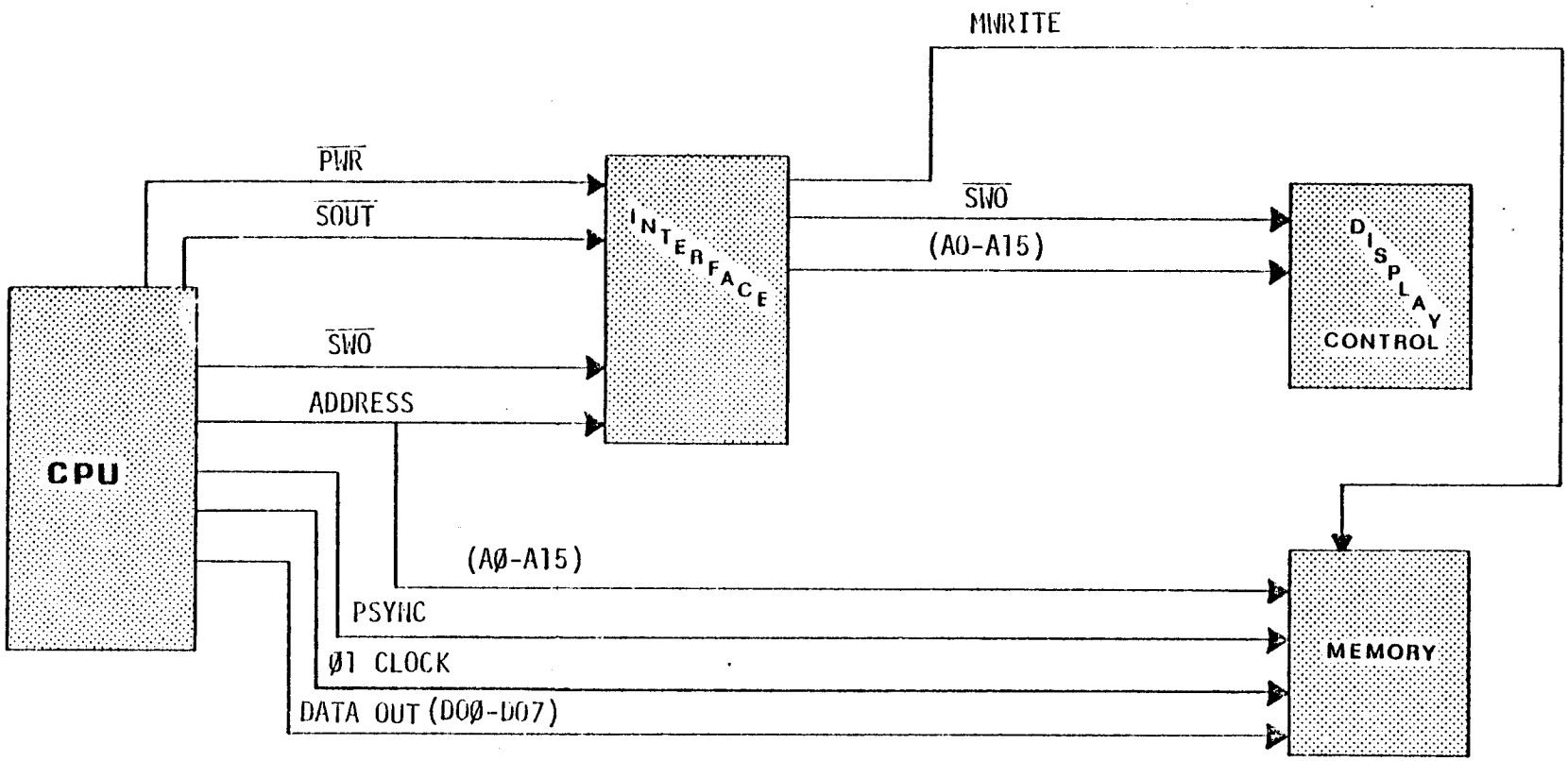

Figure 3-8. Memory Write Cycle Block Diagram

3-23. MEMORY WRITE CYCLE DETAILED OPERATION

The following paragraphs describe the Memory Write Cycle operation in detail. Refer to Figure 3-9, Memory Write Cycle Timing, during the explanation. The Memory Write Cycle operation (M4) requires three Ø1 and Ø2 clock pulses. Each period performs a certain operation as described in the following paragraphs.

During the latter portion of T1, several outputs are generated by the CPU 8080 IC (Figure 3-14); Address data AØ through A15 (zone B8), status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data contains the memory storage location address (ex. 000 200_8) which is applied to the memory card via the bus through non-inverting bus drivers U, P, and N (zone B9) on the CPU in order to enable the memory. The address data (AØ-A15) is also applied through inverters P, W, and X on the Interface Card (Figure 3-15, sheet 1, zone B5) and presented to the Display/Control card. The AØ through A15 signals present on the Display/Control card (Figure 3-16, sheet 3, zones A9-A5) light the appropriate AØ through A15 LEDs, indicating the memory location address. The DØ through D7 data is applied to K on the CPU (Figure 3-14, zone B5) through the bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7), conditioning F to generate a signal during T2.

During the beginning of T2, a LOW $\overline{STSTB}$ (zone B7) is generated from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5) allowing the status data DØ through D7 to be stored into K. The status data present at the output of K indicates a write output operation is being performed. However, the distinction of whether the data from the CPU is being transferred to a memory or an external device is determined by the status of the SOUT signal (zone A5). During a Memory Write Cycle, the SOUT signal is LOW and applied to the Interface Card (Figure 3-15, sheet 2). The SOUT signal is inverted HIGH by V and applied to pin 2 of NAND gate A (zone C3).

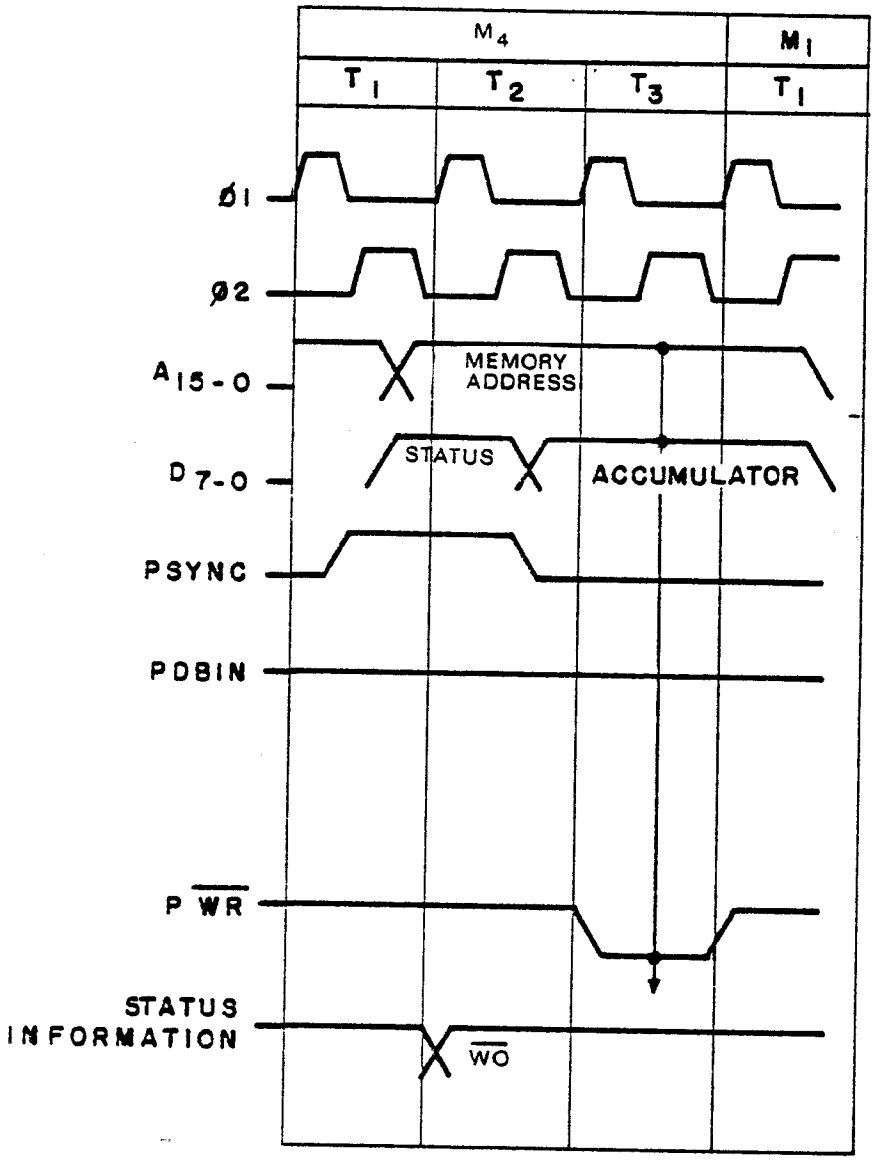

Figure 3-9. Memory Write Cycle Timing.

The $\overline{SWO}$ output from K is presented on pin 97 of the bus (zone A4) through non-inverting bus driver X as a LOW. The $\overline{SWO}$ signal is applied through inverter M on the Interface Card (Figure 3-15, sheet 2, zone B6) and presented to the Display/ Control card as SWO. The SWO signal present on the Display/ Control card lights the WO LED (Figure 3-16, zone C3) on the front panel of the 8800b, indicating data is being transferred to memory from the CPU.

At the beginning of T3, the CPU data is transferred to the memory via the bus. The CPU data out (DOØ through DO7) is applied to the bus (zone C1) through bi-directional gates D and E ($\overline{CS}$ and $\overline{DIEN}$ are LOW) and non-inverting bus drivers M and W (zones C7 and C3). The bus data is presented to memory and written in by the MWRITE signal.

After the CPU data is settled on the bus and presented to memory, a $\overline{WR}$ signal (zone C8) is generated LOW by M. The $\overline{WR}$ signal is applied to pin 77 (zone D1) of the bus through non-inverting bus driver V (zone D8) as $\overline{PWR}$. The $\overline{PWR}$ signal is inverted HIGH by U on the Interface Card (Figure 3-15, sheet 2, zone B3) and applied to pin 1 of NAND gate A (zone C3), enabling pin 6 LOW ($\overline{SOUT}$ is HIGH on pin 2). The LOW at pin 6 forces the output of NOR gate A (zone C2) HIGH which is applied to pin 68 of the bus through non-inverting bus driver H (zone B2) as MWRITE. The MWRITE signal allows the memory to store the CPU data in the addressed memory location, thus completing the CPU to memory data transfer.

3-24. MEMORY TO CPU DATA TRANSFER

A Memory to CPU data transfer is accomplished whenever an instruction is encountered to perform this operation. For example, a load accumulator LDA (072_8) instruction requires the specified addressed memory location to transfer its contents to the accumulator in the CPU. The LDA instruction was fetched during M1 and the specified memory location determined during the memory read cycles, M2 and M3. The memory data is transferred to the CPU by an additional Memory Read Cycle operation (M4). The M4 operation

requires the CPU to output the specified addressed memory location to memory, allowing the data in the specified addressed memory location to be transferred to the CPU in an identical manner as M2.

For a detailed operation description of the M2 cycle, refer to Paragraph 3-17. Note as you read the description that the specified memory address location is presented to memory on the fifteen individual address lines, allowing that location to transfer its data to the CPU.

3-25. CPU TO EXTERNAL DEVICE DATA TRANSFER

A CPU to External Device data transfer is accomplished when an output instruction (323_8) is fetched from a memory location during M1, and the external device number (XXX_8) is read from a memory location during M2 by the CPU. The data from the CPU is transferred to the external device by an Output Write Cycle operation (M3).

3-26. OUTPUT WRITE CYCLE BASIC OPERATION (Figure 3-10)

The Output Write Cycle operation will allow the CPU to output data to an external device. After completion of the Memory Read Cycle (M2), the program counter is not incremented until the completion of the Output Write Cycle. Several signals are generated by the CPU in order to transfer the data to the external device.

The SOUT and PSYNC external device ADDRESS (XXX_8) number, consisting of sixteen individual outputs (AØ-A7) from the CPU, is presented to the external device (I/O) to condition the I/O card. With the I/O conditioned, a $\overline{PWR}$ signal from the CPU allows the I/O to transfer the CPU data via the DATA OUT (DOØ-DO7) lines to the external device. The $\overline{SWO}$ output from the CPU is presented to the Display/Control through the Interface to light the WO (write output) LED on the 8800b front panel. The SOUT and AØ through A15 outputs are applied to the Display/Control through the Interface to light the OUT output and ADDRESS LEDs on the 8800b front panel.

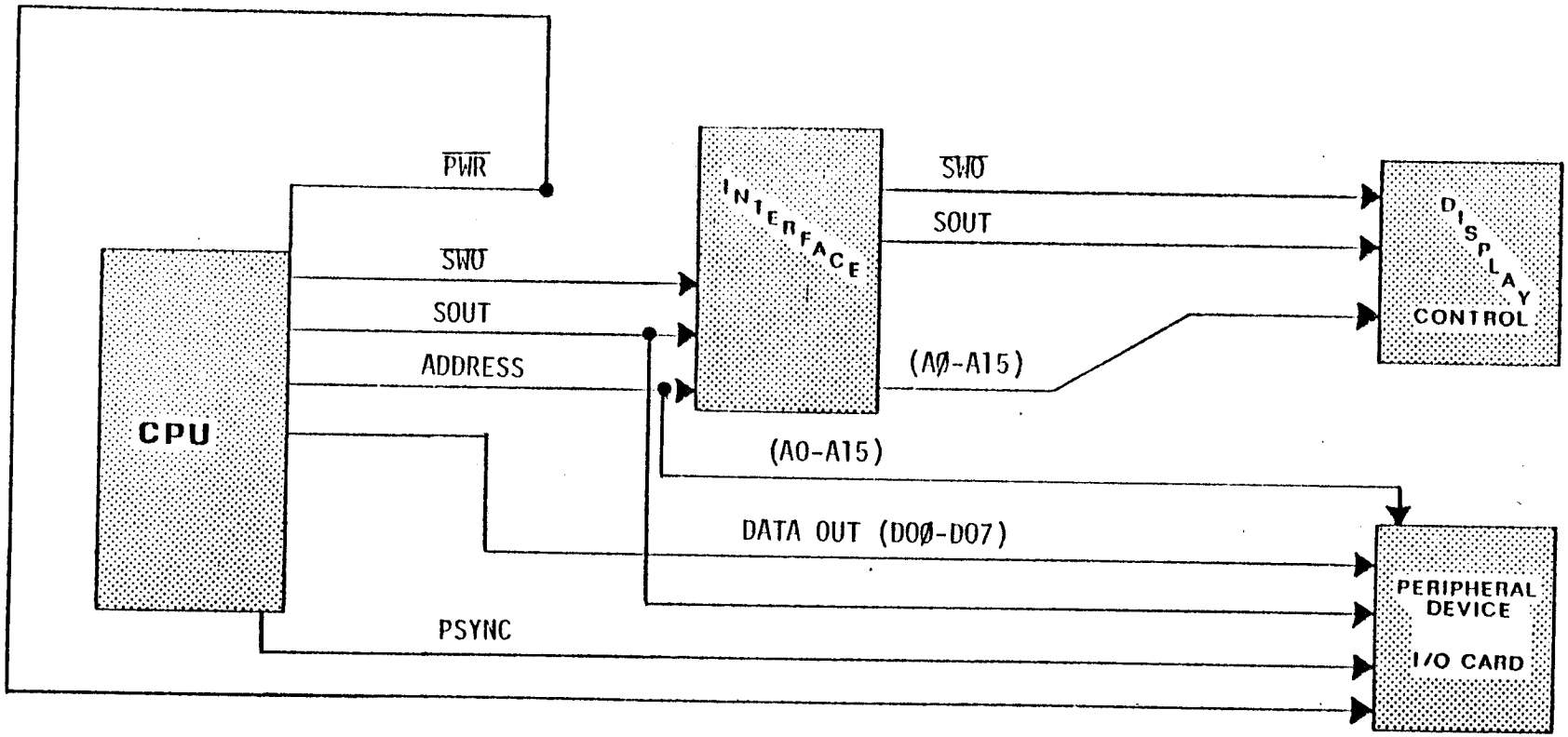

Figure 3-10. Output Write Cycle Block Diagram

3-27. OUTPUT WRITE CYCLE DETAILED OPERATION

The following paragraphs describe the Output Write Cycle operation in detail. Refer to Figure 3-11, Output Write Cycle Timing, during the explanation. The Output Write Cycle operation (M3) requires three Ø1 and Ø2 clock pulses. Each clock period performs a certain operation as described in the following paragraphs.

During the latter portion of T1, several outputs are generated by the CPU 8080 IC (Figure 3-14); Address data AØ through A15 (zone B8), status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data contains the external device number and is applied to the I/O card via the bus through non-inverting bus drivers U, P, and N (zone B9) on the CPU in order to enable the I/O card. The address data (AØ-A15) is also applied through inverters P, W, and X on the Interface Card (Figure 3-15, sheet 1, zone B5) and presented to the Display/Control card. The AØ through A15 signals present on the Display/Control card light the appropriate AØ through A15 LEDs, indicating the address of the external device. The DØ through D7 data is applied to K (zone B5) on the CPU through bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7) which conditions F to generate a signal during T2.

At the beginning of T2, a $\overline{STSTB}$ (zone B7) is generated LOW from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5), allowing the status data DØ through D7 to be stored into K. The status data present at the output of K conditions the I/O card to receive data from the CPU by enabling the SOUT and $\overline{SWO}$ signals.

A SOUT output from K is presented HIGH on pin 45 of the bus (zone A4) through non-inverting bus driver X. The SOUT signal is applied through inverter V on the Interface Card (Figure 3-15, zone B5) and presented to NAND gate A (zone C3) and the Display/Control card as SOUT. The $\overline{SOUT}$ signal disables NAND gate A to insure that a MWRITE output is not produced when writing data to an external

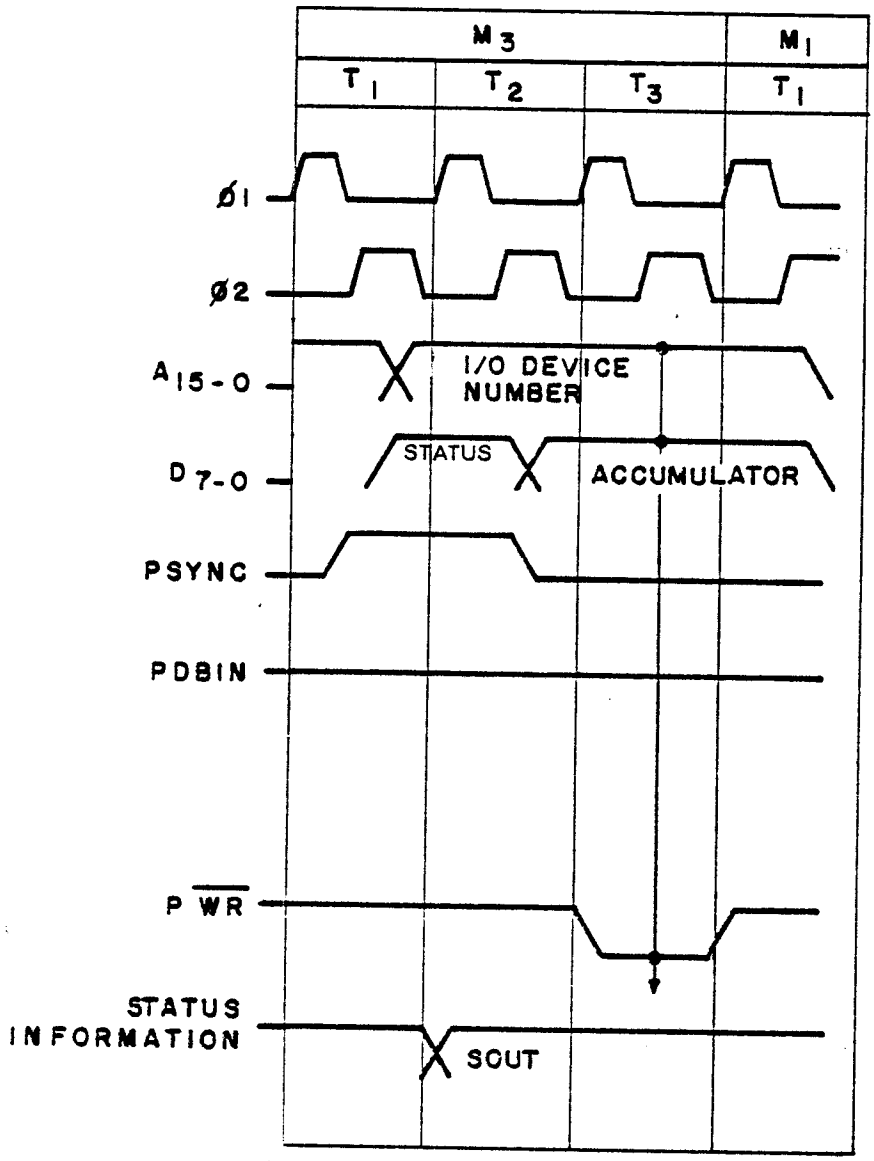

Figure 3-11. Output Write Cycle Timing.

device. It is applied to the Display/Control to light the "OUT" LED (Figure 3-16, sheet 3, zone B3), indicating data is being transferred from the CPU to an external device. The SOUT output from the CPU (Figure 3-14, zone A5) is applied to the external device I/O card in order to initiate a data transfer from the CPU during T3.

At the beginning of T3, the CPU data is transferred to the external device via the bus. The CPU data out (DOØ through DO7) is applied to the bus (zone C1) through bi-directional gates D and E ($\overline{CS}$ and $\overline{DIEN}$ are LOW) and non-inverting bus drivers M and W (zones C7 and C3). The bus data is presented to the external device and written in by the $\overline{PWR}$ signal.

After the CPU data is settled on the bus, a $\overline{WR}$ signal (zone C8) is generated LOW by M. The $\overline{WR}$ signal is applied to pin 77 (zone D1) of the bus through non-inverting bus driver V (zone D8) as $\overline{PWR}$. The $\overline{PWR}$ signal allows the external device to store the CPU data, thus completing the CPU to external device data transfer.

3-28. FRONT PANEL OPERATION

A variety of functions may be performed through the operation of the front panel: e.g. selecting a starting location for a program, examining memory locations, single stepping through a program, depositing and displaying CPU accumulator data, and depositing data into a specified memory location. Each of the functions performed on the 8800b front panel are discussed in the following paragraphs. The run operation was discussed in Paragraph 3-10.

3-29. FRONT PANEL BLOCK DIAGRAM (Figure 3-12)

The front panel switches allow the operator to assume control of the CPU. The CPU is controlled by a FRDY signal which is generated from the front panel display control circuits. The FRDY signal places the CPU in either a wait condition or a run operation.

The CPU is placed in a wait condition when the Switches and Decoding circuits sense that the RUN/STOP switch on the front panel is positioned to STOP. A STOP signal is applied to the Stop/Run

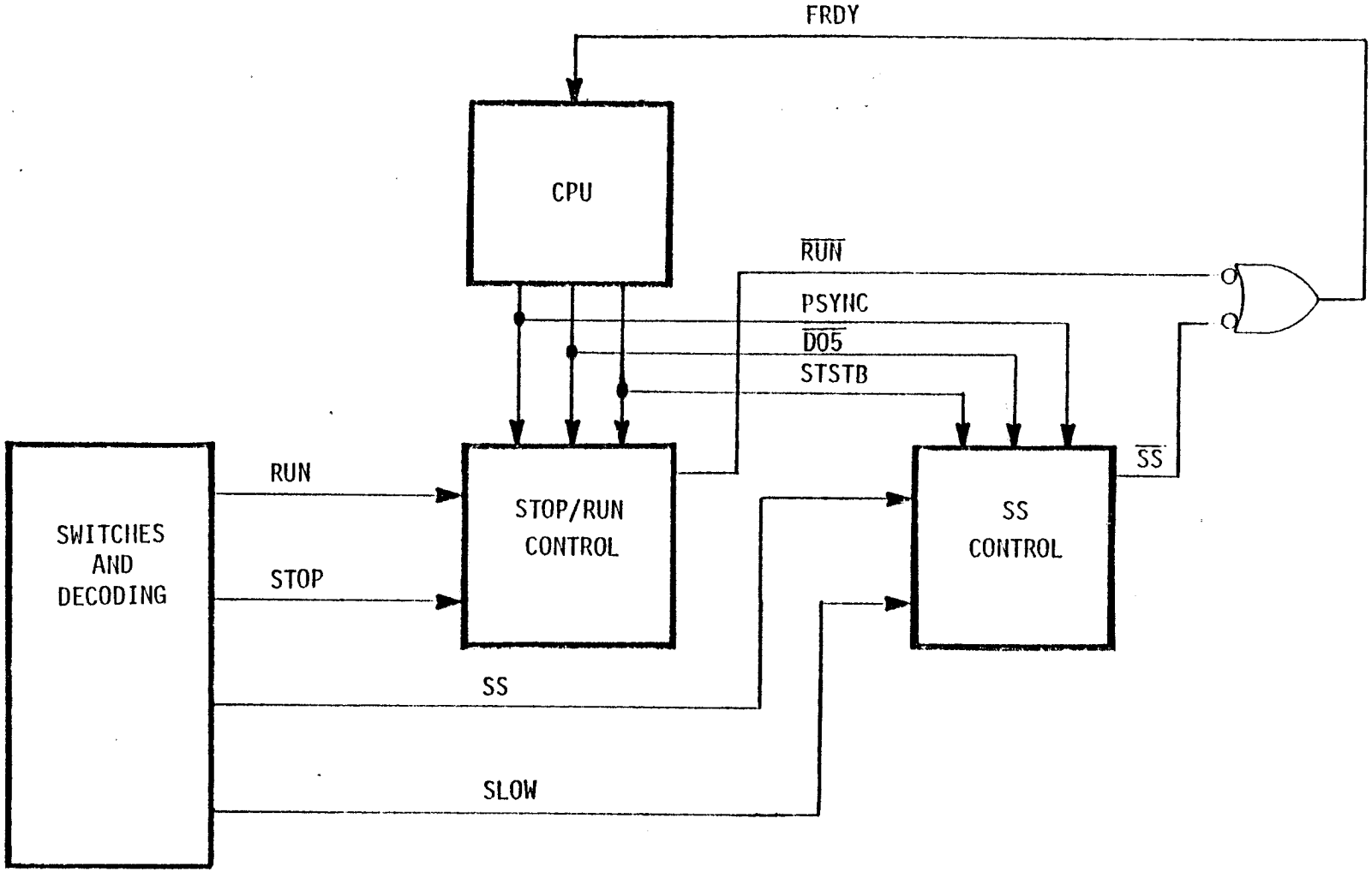

Figure 3-12. Front Panel Block Diagram

Control circuits to disable (HIGH) the $\overline{RUN}$ signal. The $\overline{RUN}$ signal forces the CPU to a wait condition by disabling (LOW) the FRDY line. The CPU will not enter a wait condition until the PSYNC, $\overline{DO5}$, and STSTB signals are presented to the Stop/Run Control circuits. The presence of these signals insures that the CPU will stop during the first machine cycle of an instruction cycle.

The CPU is placed in a single step (SS) or slow run operation by the generation of an SS or SLOW signal from the Switches and Decoding circuits. The SS or SLOW run operation allows the CPU to perform one instruction cycle. The SS signal is applied to the SS Control circuit, enabling (LOW) the $\overline{SS}$ signal. The $\overline{SS}$ signal allows the CPU to execute one instruction cycle by enabling the FRDY signal. Upon the completion of the instruction cycle, the CPU attempts to perform another instruction cycle, but the PSYNC, $\overline{DO5}$, and STSTB signals reset the SS Control circuits forcing the CPU to a wait condition.

3-30. STOP OPERATION

The stop operation allows the operator to use the switches on the 8800b front panel. The stop operation is activated when the RUN/STOP switch on the 8800b front panel is momentarily depressed to STOP.

The RUN/STOP circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A9). With the RUN/STOP switch momentarily depressed, a LOW is applied to quad latch C1, input D1. The occurrence of the next C13 clock (zone A1) causes the $\overline{Q}$ output at pin 3 of C1 (zone B9) to go HIGH which is applied to quad latch N1, input D1. The next C13 clock causes the Q output at pin 7 of N1 (zone B9) to go HIGH which is applied to the D input of M1. A HIGH present at D produces a clock pulse to set M1, stopping the CPU.

The clock pulse that sets M1 is derived from three signals: $\overline{DO5}$, $\overline{PSYNC}$, and $\overline{STSTB}$ (zone D8). The signals are enabled during machine cycle 1 (paragraph 3-14) of an 8800b instruction cycle, and their presence generates a clock to M1 (zone C9). This insures that the 8800b stops during the first machine cycle of an instruc-

tion cycle. The DO5 signal is generated by the CPU (Figure 3-14, zone C1) and presented to pin 39 of the bus as a HIGH through the bi-directional gate E (zone C7) and non-inverting bus driver W (zone C3) and applied to the Interface Card (Figure 3-15, sheet 2, zone C2). The DO5 signal is inverted by Y (zone B2) and inverted again by R1 on the Display/Control Card (Figure 3-16, sheet 2, zone D8) and applied HIGH to pin 3 of NAND gate D1 (zone C8). The PSYNC is generated by the CPU (Figure 3-14, zone D1) on pin 76 of the bus as a HIGH through non-inverting bus driver V (zone D8) and applied to the Interface Card (Figure 3-15, sheet 2, zone A3). PSYNC is inverted by U (zone B3) and R1 on the Display/Control Card (sheet 5, zone B3) and applied HIGH to pin 4 of NAND gate D1 (zone C8).

The $\overline{\text{STSTB}}$ is generated by the CPU (Figure 3-14, zone A4) to pin 56 of the bus as a LOW through non-inverting bus driver R and applied to the Interface Card (Figure 3-15, sheet 2, zone A4). The $\overline{\text{STSTB}}$ is inverted and then inverted again by the Interface Card (sheet 2, zone A4) and applied to pin 5 of NAND gate D1 on the Display/Control Card (Figure 3-16, sheet 2, zone C8) as a HIGH. These signals allow NAND gate D1 to produce a HIGH at gate P1, pin 6 (zone C8), which sets M1. The $\overline{Q}$ output of M1 goes LOW and is applied through K1 (zone A8) to enable all the front panel switches. The $\overline{Q}$ output is also presented to gate P1 which keeps a high on the CK input of M1 (zone C9), insuring that M1 remains set after the stop switch is released.

Because M1 is set, the Q output of M1 (zone C9) is HIGH, disabling the $\overline{\text{RUN}}$ and $\overline{\text{FRDY}}$ signals. The $\overline{\text{FRDY}}$ signal is applied to NAND gate C on the CPU (Figure 3-14, zone A8) through the Interface (Figure 3-15, sheet 2, zone A1) as a LOW. This inhibits the RDYIN signal at F (Figure 3-14, zone B7) which disables the READY signal to M (zone A8), thereby halting the CPU.

3-31. SINGLE STEP OPERATION

The single step operation allows the operator to increment one instruction cycle at a time. The single step operation is activated when the SINGLE STEP/SLOW switch is momentarily positioned to SINGLE STEP.

The SINGLE STEP circuits are located on the Display/Control card (Figure 3-16, sheet 1, zone A8). With the SINGLE STEP/SLOW

switch momentarily positioned to SINGLE STEP, a LOW is presented to pin 1 of gate P1 (zone C8). The LOW input at D1 generates a clock pulse which sets M1 (zone A7), producing a LOW at the $\overline{Q}$ output of M1. The LOW output is applied to pin 13 of gate P1 (zone C9), enabling the $\overline{FRDY}$ signal (zone D9). The CPU performs one instruction cycle with $\overline{FRDY}$ enabled. At the completion of the instruction cycle, the $\overline{DO5}$, $\overline{PSYNC}$, and $\overline{STSTB}$ input (zone D8) enable NAND gate T1, pin 12 (zone C6), LOW which produces a LOW at the output of inverter J1 (zone C6). The LOW clears the M1 flip-flop, thereby ending the first single step operation. Additional single step operations are enabled by momentarily depressing the SINGLE STEP/SLOW switch to SINGLE STEP.

The DO5 input is applied to pin 1 of NAND gate T1 through jumpers JE and JF (zone D7). If this jumper is removed, pin 1 of NAND gate is always HIGH. Under this condition, the PSYNC and $\overline{STSTB}$ signals would reset M1 after each machine cycle.

3-32. SLOW OPERATION

The slow operation is very similar to the single step operation except the slow operation allows the 8800b to execute instruction cycles at a very slow rate (786 milliseconds vs. 3 milliseconds normal operation).

The slow circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A8). When the SINGLE STEP/SLOW switch is positioned to SLOW, a HIGH is presented to pin 9 of NAND gate P1 (zone B7). The HIGH at pin 9 enables the C18 clock (zone D7) from a 24-bit counter (sheet 1, zone D1) through NAND gate P1 (sheet 2, zone B7). This clock enables pin 12 of gate D1 (zone C8) HIGH, providing a clock pulse to set M1 (zone A7), producing a LOW at the $\overline{Q}$ output, M1. The LOW output is applied to pin 13 of gate P1 (zone C9), enabling the $\overline{FRDY}$ signal (zone D9). With $\overline{FRDY}$ enabled, the CPU performs one instruction cycle. At the completion of the instruction cycle, the $\overline{DO5}$, $\overline{PSYNC}$, and $\overline{STSTB}$ input (zone D8) enable NAND gate T1, pin 12 (zone C6), LOW which produces a LOW at the output of inverter J1 (zone C6). This LOW clears the M1 flip-flop, ending the first single step operation. If the SINGLE STEP/

SLOW switch is still positioned to SLOW, another instruction cycle operation is performed. Otherwise, the machine halts. If jumpers JE and JF (zone C7) are removed, the machine may not stop at the beginning of an instruction cycle.

3-33. RESET OPERATION

The reset operation allows the operator to reset the CPU at anytime during machine operation. The reset is activated when the RESET/EXT CLR switch on the front panel is positioned to RESET.

The reset circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A2). With the RESET/EXT CLR switch momentarily positioned to RESET, a PRESET signal (zone D3) is applied to the Interface (Figure 3-15, sheet 2, zone D1) as a HIGH. The HIGH is inverted by R and applied to pin 75 (zone A1) of the bus through non-inverting bus driver N (zone B1). The CPU receives the $\overline{\text{PRESET}}$ signal and inverts it twice through G and B (Figure 3-14, zone B6). The output of B is applied to the clock generator F $\overline{\text{RESIN}}$ (reset in) input (zone B7), producing a RESET output to the 8080 (M).

3-34. PROTECT AND UNPROTECT OPERATION

The protect/unprotect operation either prevents any new data from being written into a particular region of memory (protect) or allows new data to be written into a particular region of memory (unprotect). The protect/unprotect operation is controlled by the positioning of the PROTECT/UNPROTECT switch on the front panel.

The protect/unprotect circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A1). With the PROTECT/UNPROTECT switch positioned to either PROTECT or UNPROTECT, a $\overline{\text{PROTECT}}$ or $\overline{\text{UNPROTECT}}$ signal (zone D3) is applied to the Interface as a LOW. The LOW is inverted by R (Figure 3-15, sheet 2, zone B6) and applied to pin 70 and 20 on the bus to condition the memory. These signals are used to set or reset the protect/unprotect circuits on the addressed memory board.

3-35. PROGRAMMABLE READ ONLY MEMORY (PROM) CIRCUIT

The PROM circuit on the Display/Control Card is used when one of the following operations is performed: Examine, Examine Next, Deposit, Deposit Next, Accumulator Display, Accumulator Load, Accumulator Input and Accumulator Output. Each of the functions requires a program operation that is stored in the PROM. Access to these programs is determined by the type of function to be performed. The PROM operation is similar for each function, therefore two functions are discussed in detail.

3-36. PROM BLOCK DIAGRAM (Figure 3-13)

The PROM circuit contains eight individual programs which are used in conjunction with the following switches: EXAMINE/EX NEXT, DEPOSIT/DEP NEXT, ACCUMULATOR DISPLAY/LOAD, and ACCUMULATOR INPUT/OUTPUT. Activating any of these switches produces a specific binary number on the RA4, RA5, RA6, and RA7 lines (MSBs) from the Switches and Decoding circuit. At the same time the RA4 through RA7 data is generated, a RESET signal is applied to the 4-Bit Counter, conditioning the RAØ, RA1, RA2, and RA3 outputs (LSBs) to zero. The RAØ-RA7 signals are applied to the PROM, and they represent an 8-bit starting address location. There are eight different starting address locations which correspond to the eight different front panel switch settings (refer to Table 3-2). Any of the eight different starting address locations are always even because of the resetting of the 4-Bit Counter.

The PROM circuit outputs a DATA OUT (RDØ-RD7) signal, consisting of eight individual lines, to either the Control Latch or the non-inverting bus driver F. The DATA OUT is transferred to one of these two circuits by the status of the RAØ signal from the 4-Bit Counter. When the RAØ signal is LOW, representing a PROM even address, the Control Latch receives the data. The even addresses of the PROM contain data that is used to enable the Control Latch output lines (S1-S8). After the Control Latch receives the PROM data, a CLOCK signal increments the 4-Bit Counter to an odd PROM address location. During an odd PROM address cycle, the CPU will execute one machine cycle (assuming the S8 bit has been set in the Control Latch). If the cycle is a memory read cycle, an instruction

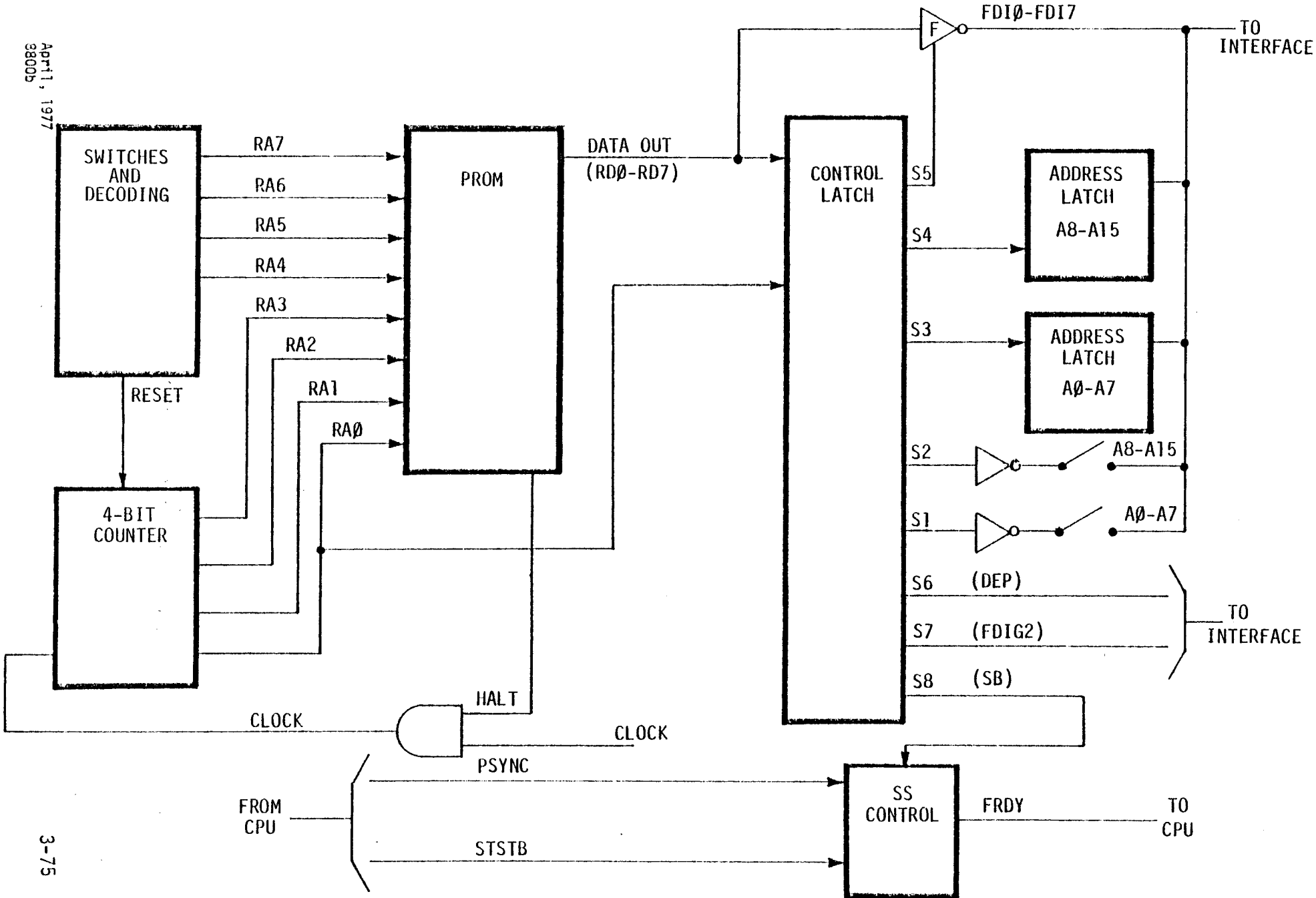

Figure 3-13. PROM Block Diagram

TABLE 3-2. PROM Programs

Front Panel Operations	PROM Address	PROM DATA	Function
Examine	160*	013*	Set S5, S7, S8
	161	303	Jam Jump Instruction to CPU
	162	203	Set S1, S7, S8
	163	000	Jam AØ-A7 switch data to CPU
	164	103	Set S2, S7, S8
	165	000	Jam A8-A15 switch data to CPU
	166	000	Clear control latch
	167	177	Stop
Examine Next	260	013	Set S5, S7, S8
	261	000	Jam NOP instruction to CPU
	262	000	Clear control latch
	263	177	Stop
Deposit	320	206	Set S1, S6, S7
	321	000	Put AØ-A7 switch data and MWRITE pulse on bus
	322	000	Clear control latch
	323	177	Stop
Deposit Next	340	013	Set S5, S7, S8
	341	000	Jam NOP instruction to CPU
	342	206	Set S1, S6, S7
	343	000	Put AØ-A7 switch data and MWRITE pulse on bus
	344	000	Clear control latch
	345	177	Stop
Display Accumulator	060	013	Set S5, S7, S8
	061	323	Output Instruction
	062	013	Set S5, S7, S8

*All PROM address and data information is octal.

TABLE 3-2. PROM Programs - Continued

Front Panel Operations	PROM Address	PROM DATA	Function
	063*	377*	Jam front panel address to CPU
	064	001	Set S8
	065	000	Data in accumulator is transferred to the DØ-D7 LEDs
	066	013	Set S5, S7, S8
	067	303	Jam jump instruction to CPU
	070	043	Set S3, S7, S8
	071	000	Jam AØ-A7 latch data to CPU
	072	023	Set S4, S7, S8
	073	000	Jam A8-A15 latch data to CPU
	074	000	Clear control latch
	075	177	Stop
Accumulator Deposit	220	013	Set S5, S7, S8
	221	333	Jam input instruction to CPU
	222	013	Set S5, S7, S8
	223	376	Jam front panel address to CPU
	224	203	Set S1, S7, S8
	225	000	Data in accumulator is transferred to CPU
	226	013	Set S5, S7, S8
	227	303	Jam jump instruction to CPU
	230	043	Set S3, S7, S8
	231	000	Jam AØ-A7 latch data to CPU
	232	023	Set S4, S7, S8
	233	000	Jam A8-A15 latch data to CPU
	234	000	Clear control latch
	235	177	Stop
Input from external device selected by ADDRESS switches A8-A15	300	013	Set S5, S7, S8
	301	333	Jam input instruction to CPU
	302	103	Set S2, S7, S8
	303	000	Jam A8-A15 switch data to CPU

*All PROM address and data information is octal.

TABLE 3-2. PROM Programs - Continued

Front Panel Operations	PROM Address	PROM DATA	Function
	304*	001*	Set S8
	305	000	Data in accumulator is transferred to specific I/O device
	306	013	Set S5, S7, S8
	307	303	Jam jump instruction to CPU
	310	043	Set S3, S7, S8
	311	000	Jam AØ-A7 latch data to CPU
	312	023	Set S4, S7, S8
	313	000	Jam A8-A15 latch data to CPU
	314	000	Clear control latch
	315	177	Stop
Output from external device selected by ADDRESS switches A8-A15	240	013	Set S5, S7, S8
	241	323	Jam output instruction to CPU
	242	103	Set S2, S7, S8
	243	000	Jam A8-A15 switch data to CPU
	244	001	Set S8
	245	000	Data is transferred from specific I/O device to accumulator
	246	013	Set S5, S7, S8
	247	303	Jam jump instruction to CPU
	250	043	Set S3, S7, S8
	251	000	Jam AØ-A7 latch data to CPU
	252	023	Set S4, S7, S8
	253	000	Jam A8-A15 latch data to CPU
	254	000	Clear control latch
	255	177	Stop

*All PROM address and data information is octal.

byte is supplied to the CPU on the FDIØ-FDI7 lines.

The instruction data at the odd PROM address is transferred to the CPU through the Interface from five different sources. The source is determined by the output control lines S1 through S5 from the Control Latch.

The S1 and S2 control lines enable the front panel switch data, AØ through A15, to the Interface. The S3 and S4 control lines enable the Address Latch data, AØ through A15, to the Interface. The S5 control line enables the DATA OUT (RDØ-RD7) from the PROM to the Interface.

The data present at the Interface is applied to the CPU by output control lines S7 and S8 from the Control Latch. The S7 control line allows the Interface to apply the instruction data to the CPU, and the S8 control line enables the FRDY signal. The FRDY signal allows the CPU to receive the instruction data and execute one machine cycle. After the completion of the machine cycle, the PSYNC and STSTB signals from the CPU reset the SS Control circuit. The S6 control line is enabled from the Control Latch to allow data to be deposited into memory. Upon the completion of a PROM program, a HALT signal is generated by the PROM, disabling the CLOCK signal to the 4-Bit Counter.

3-37. EXAMINE OPERATION

The examine operation allows the operator to examine a memory location by using the ADDRESS switches on the front panel. Refer to Table 3-2 during the explanation. The examine operation is activated when the EXAMINE/EXAMINE NEXT switch is momintarily positioned to EXAMINE.

The EXAMINE circuit is located on the Display/Control card (Figure 3-16, sheet 2, zone B7). With the EXAMINE/EXAMINE NEXT switch momentarily positioned to EXAMINE, a LOW is generated at pin 6 of inverter V1 (zone B7) and a HIGH at the output of the remaining V1 and Z1 inverters (zones B6 through B3). The LOW output is applied to pin 6 of gate X1 which generates a HIGH to set L1 (zone D4). The $\overline{\text{RC-CLR}}$ (LOW) and AL-STB (HIGH) outputs

from L1 reset a 4-bit binary counter to zero (sheet 2, zone A9) and strobes the current address data into data latches B1 and T1 (zone B6). The L1 latch is cleared by the $\overline{C6}$ signal from the 24-bit binary counter (sheet 1, zone D3). The LOWs and HIGHs from the inverters are presented as RA7 through RA4 inputs to the PROM (sheet 1, zone B9).

The RAØ through RA7 inputs to the PROM (zone B9) represent an address location (160_8). This location is the beginning of the examine program stored in the PROM. The data in address location 160_8 is presented on the RDOØ through RDO7 outputs (013_8) and applied to data latch A (zone D8). After the 4-bit binary counter (zone B9) is LOW during the even addresses (RAØ=0), and a control strobe (CS) to DS2 (zone C8) is generated, the data present at latch A is stored by the A output.

The CS strobe is produced by the 24-bit counter outputs C6, C7, and $\overline{C8}$ (zone D3). When the C6, C7, and $\overline{C8}$ counter outputs are HIGH, NAND gate V (zone D5) is enabled LOW, and CS (zone D6) is applied HIGH to the DS2 input of data latch A (zone C8). With DS2 and $\overline{DST}$ enabled, the RDØ through RD7 data (013_8) is latched into A. The 013_8 data enables outputs S5, S7, and S8 (zone D7) HIGH. Output S5 is inverted LOW by A1 (zone A6), enabling inverting bus drivers R and S. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gates J (zone D6). With the PROM data stored in latch A and the associated circuits conditioned, NAND gate Z (zone A7) produces a clock pulse to INP A of the 4-bit counter (zone A8). When C8 goes HIGH from the 24-bit counter (zone D3), the 4-bit counter, A output, goes HIGH which addresses PROM location 161_8.

The data in address location 161_8 is present on the RDØ through RD7 outputs 303_8. The 303_8 data is transferred to the Interface on the FDIØ-FDI7 (zone C2) outputs through enabled inverting bus drivers R and S (zone A6). The data is not stored in Latch A because the A output (zone B9) of the 4-bit counter is HIGH (odd address RAØ=1), disabling the $\overline{DST}$ input (zone C7). The A output is applied to pins 1 and 5 of NAND gates J (zone D6).

The $\overline{FDI\emptyset}$ through $\overline{FDI7}$ data presented to the Interface Card (Figure 3-15, sheet 2, zone D8) represents a jump instruction to be stored in the CPU. The CPU cannot receive this instruction and execute it until the $\overline{FDIG2}$ (zone D7) signal is LOW, and the CPU is released from the wait condition generated when the CPU was stopped. The following operation allows the CPU to receive the jump instruction.

When the C6, C7, and $\overline{C8}$ outputs of the 24-bit counter on the Display/Control (Figure 3-16, sheet 1, zone D3) are HIGH, another CS signal (zone D6) is generated. The CS signal allows NAND gate J, pins 6 and 12, to produce $\overline{SB}$ (zone D4) and $\overline{FDIG2}$ (zone C2) signals.

The $\overline{SB}$ signal is applied to pin 13 of gate D1 (sheet 2, zone C8) as a LOW, producing a HIGH clock pulse to set M1 (zone C7). The $\overline{Q}$ output of M1 is applied to pin 13 of NOR gate P1 and inverter R1 (zone D9), allowing the $\overline{FRDY}$ signal to release the CPU from its wait condition.

The $\overline{FDIG2}$ signal is applied to pin 12 of NOR gate B (Figure 3-15, sheet 2, zone C7) on the Interface as a LOW which enables NAND gate B, pin 6, LOW (PDBIN is HIGH because the CPU is in a wait condition). The LOW enables the non-inverting drivers F (zone B7), allowing the PROM data (303_8) to be applied to M on the CPU through bi-directional gates D and E on the CPU (Figure 3-14, zone C7). Because the READY line to M (zone A8) is HIGH, the CPU inputs the 303_8 data which is interpreted by the CPU as a jump instruction. After the completion of the machine cycle, the $\overline{PSYNC}$ and $\overline{DO5}$ signals (sheet 2, zone D8) are inverted by R1 and applied to pins 11 and 10 of NAND gate T1 (zone D6). These signals and $\overline{SB}$ (zone D8) enable T1 which generates a clear to M1 (zone C7), halting the CPU.

The CPU contains a jump instruction but no information as to where to jump. The remaining part of the examine operation allows the ADDRESS switch data to be read into the CPU from the front panel in order for the CPU to jump to that address. NAND gate Z (sheet 1, zone A7) produces another clock pulse to INP A of the 4-bit counter. When C8 goes HIGH and returns LOW (zone D3), the 4-bit counter increments to an even PROM address 162_8.