The data in address location 162_8 is present on the RDØ through RD7 outputs (203_8) and applied to data latch A (zone D8). The data present at latch A is stored by the LOW A output (zone B9) during even addresses (RAØ=0) and the generation of the CS strobe (C6, C7, and $\overline{C8}$ HIGH). The 203_8 data enables outputs S1, S7, and S8 (zone D7) HIGH. Output S1 is applied through inverters Y and W (zone C4) to the AØ through A7 switches (open switch HIGH, closed switch LOW), and the switch information is presented to the Interface as $\overline{FDIØ}$ through $\overline{FDI7}$. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gate J (zone D6) and are used to generate the $\overline{FDIG2}$ and $\overline{SB}$ signals as described in the jump instruction transfer. With the data presented to the Interface Card and the associated circuits conditioned, NAND gate (zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 163_8.

The data in address 163_8 is not stored in latch A because it is an odd address. However, the A output (zone B9) is applied to pins 1 and 5 of NAND gates J (zone D6) as a HIGH, allowing the CS signal to produce the $\overline{SB}$ and $\overline{FDIG2}$ outputs. The $\overline{SB}$ and $\overline{FDIG2}$ signals allow the transfer of the first eight address data bits (address switches AØ-A7) to the CPU, and the operation is identical to the jump instruction.

After the CPU receives the eight address bits, the 4-bit binary counter is incremented to address 164_8. The data in 164_8 (01000110 - 103_8) is stored in latch A (zone D7) because it is an even address. The 103_8 data enables S2, S7, and S8 (zone D7) HIGH. Output S2 is applied to inverter A1 (zone C6), gate Z (zone C5), and inverters W and U (zone C4) to the A8 through A15 address switches. The switch information is presented to the Interface as $\overline{FDIØ}$ through $\overline{FDI7}$. Outputs S7 and S8 condition NAND gates J (zone D6) and are used to generate $\overline{SB}$ and $\overline{FDIG2}$ during the next address. With the data present to the Interface and the associated circuits conditioned, NAND gate Z (zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 165_8.

Address 165_8 operation is the same as address 163_8, allowing the A8 through A15 address data to be stored in the CPU. After

the CPU receives the second byte of the address, it executes a jump to that address. Address 166_8 clears the data latch A (zone D7) and allows the CPU to address memory (Figure 3-14, zone B9). The memory presents the addressed memory location data to the CPU via data input lines DIØ through DI7 (zone B1). The data is enabled through inverters Y, S, L, and J (zone B4) and non-inverters P, W (zone C3) to the Interface (Figure 3-15, sheet 1, zone B1). The data is enabled through the G data latch (sheet 3, zone B4) to the Display/Control (Figure 3-16, sheet 3, zone D1) and displayed on the LEDs. The G latch (sheet 3, zone B4) is enabled because the $\overline{\text{RUN}}$ signal (zone A6) is HIGH, producing a HIGH at input MD of the data latch.

While the memory data was being displayed, the 4-bit binary counter (Figure 3-16, sheet 1, zone A9) is incremented to address 167_8. The data in 167_8 (01111111 - 177_8) is applied to NAND gate N (zone B7), producing a HIGH at gate Z (zone B8). The HIGH at gate Z disables NAND gate Z (zone A8), inhibiting any following clock pulses to the 4-bit binary counter, thus ending the examine operation.

3-38. ACCUMULATOR DISPLAY OPERATION

The accumulator (ACC) display operation allows the operator to monitor the contents of the CPU accumulator. Refer to Table 3-1, PROM Programs, during the explanation. The ACC display operation is activated when the ACC DISPLAY/ACC DEPOSIT switch is momentarily positioned to ACC DISPLAY.

The ACC DISPLAY circuit is located on the Display/Control card (Figure 3-16, sheet 2, zone A5). With the ACC DISPLAY/ACC DEPOSIT switch momentarily positioned to ACC DISPLAY, a LOW is generated at pins 8 and 10 of inverter V1 (zone B5), and a HIGH is generated at the output of the remaining V1 and Z1 inverters (zones B7 through B3). The LOW outputs are applied to pins 6 and 5 of gate X1 which generates a HIGH to set L1 (zone D4). The $\overline{\text{RC-CLR}}$ (LOW) and AL-STB (HIGH) outputs from L1 reset a 4-bit binary counter to all zeros (sheet 1, zone A9) and strobe the address in the P counter into data latches B1 and T (zone B6). The P counter address data is stored because the P counter increments during the accumulator display operation. The original P

count is saved and restored in the CPU after the ACC display operation is complete. The L1 latch is cleared by the $\overline{C6}$ signal from the 24-bit binary counter (sheet 1, zone D3). The LOW and HIGHs from the inverters are presented as RA7 through RA4 inputs to the PROM (sheet 1, zone B9). An $\overline{ACC\ DSP}$ signal (zone D3) is also applied LOW to the Interface (Figure 3-15, sheet 3, zone A1), producing a LOW to the MD input of data latch G (zone A4).

The RAØ through RA7 inputs to the PROM (zone B9) represent an address location (060_8). This location is the beginning of the ACC display program stored in the PROM. The data in address location 060_8 is presented on the RDØ through RD7 outputs (013_8) and applied to data latch A (zone D8). The data present at latch A is stored by the LOW A output (zone B9) during the even addresses (RAØ=0) and the generation of a control strobe (CS) to DS2 (zone C8).

The CS strobe is produced by the 24-bit counter outputs C6, C7, and $\overline{C8}$ (zone D3). When the C6, C7, and $\overline{C8}$ counter outputs are HIGH, NAND gate V (zone D5) is enabled LOW, the CS (zone D6) is applied HIGH to the DS2 input (zone C8). The RDØ through RD7 data (013_8) is latched into A with DS2 and $\overline{DS1}$ enabled. The 013_8 data enables outputs S5, S7, and S8 (zone D7) HIGH. Output S5 is inverted LOW by A1 (zone A6), enabling inverting bus drivers R and S. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gates J (zone D6). With the PROM data stored in latch A and the associated circuits conditioned, NAND gate Z (zone A7) is enabled, producing a clock pulse to INP A of the 4-bit counter (zone A8). When C8 goes HIGH from the 24-bit counter (zone D3), the 4-bit counter A output goes HIGH which addresses PROM location 061_8.

The data in address location 061_8 is present on the RDØ through RD7 outputs (323_8). The 323_8 data is transferred to the Interface on the $\overline{FDIØ}$-$\overline{FDI7}$ (zone C2) outputs through enabled inverting bus drivers R and S (zone A6). The data is not stored in latch A because the A output (zone B9) of the 4-bit counter is HIGH (odd address), disabling the $\overline{DS1}$ input (zone C7). The A output is applied to pins 1 and 5 of NAND gates J (zone D6).

The FDIØ through $\overline{FDI7}$ data presented to the Interface (Figure 3-15, sheet 2, zone D8) represents an output instruction to be stored in the CPU. The CPU cannot receive this instruction and

execute it until the FDIG2 (zone D7) signal is LOW, and the CPU is released from the wait condition generated when the CPU was stopped. The following operation allows the CPU to receive the output instruction.

When the C6, C7, and $\overline{C8}$ outputs of the 24-bit counter on the Display/Control (Figure 3-16, sheet 1, zone D3) are HIGH, another CS signal (zone D6) is generated. The CS signal allows NAND gate J, pins 6 and 12, to produce a $\overline{FDIG2}$ (zone C2) and $\overline{SB}$ (zone D4) signal.

The $\overline{SB}$ signal is applied to pin 13 of gate D1 (sheet 2, zone C8) as a LOW which produces a HIGH clock pulse to set M1 (zone C7). The $\overline{Q}$ output of M1 is applied to gate P1 and inverter R1 (zone D9), allowing the $\overline{FRDY}$ signal to release the CPU from its wait condition.

The $\overline{FDIG2}$ signal is applied to pin 12 of gate 13 (Figure 3-15, sheet 2, zone C7) as a LOW which enables NAND gate B, pin 6, LOW. The LOW allows the PROM data (323_8) to be applied to M on the CPU through bi-directional gates D and E on the CPU (Figure 3-14, zone C7). Because the READY line to M (zone A8) is HIGH, the CPU inputs the 323_8 data which is interpreted as an output instruction. After the completion of the machine cycle, the $\overline{PSYNC}$ and $\overline{D05}$ signals (Figure 3-14, sheet 2, zone D8) are inverted by R1 and applied to pins 11 and 10 of NAND gate T1 (zone D6). These signals and $\overline{SB}$ (zone D8) enable T1 which generates a clear to M1 (zone C7), halting the CPU.

The CPU contains an output instruction but no information as to where to output data. The next part of the ACC display operation allows the CPU to output data to the front panel data LEDs (DØ through D7). NAND gate Z (sheet 1, zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing 4-bit counter (zone A8) to address 062_8.

The data in address location 062_8 is present on the RDØ through RD7 outputs (013_8) and stored in data latch A (zone D8) in the same manner as address 060_8. This insures that the S5, S7, and S8 outputs (zone D7) are enabled as in address 060_8. After the completion of this operation, NAND gate Z (zone A7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit counter

(zone A8) to address 063_8.

The data in address location 063_8 is present on the RDØ through RD7 outputs (377_8) which is the I/O channel number for the front panel. The 377_8 data is transferred to the CPU in the same manner as the output instruction at address 061_8. The 377_8 data allows the CPU to address the front panel and output the accumulator data to the DØ through D7 LEDs on the front panel. With the output instruction and front panel address number stored in the CPU, NAND gate Z (zone B7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit binary counter (zone A8) to address 064_8.

The data in address location 064_8 is present to the RDØ through RD7 outputs (001_8) and stored in data latch A (zone D8). The 001_8 data enables output S8 (zone D7) HIGH which is used during address 065_8. After the data in address location 064_8 is stored in data latch A, NAND gate Z (zone B7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit binary counter (zone A8) to address 065_8.

Address 065_8 enables the $\overline{SB}$ signal (zone D4) as described in address 061_8. The CPU performs one machine cycle with $\overline{SB}$ enabled. During the one machine cycle, the CPU outputs address 377_8 on the AØ - A7 and A8 - A15 address lines to the bus (Figure 3-14, zone B9). The CPU also outputs accumulator data through bi-directional gates D and E (zone C7) and non-inverting bus drivers P and W (zone C3) to the data out (DOØ-DO7) bus. The address data (377_8) enables NAND gates L on the Interface board (Figure 3-15, sheet 3, zone C6) LOW. The LOWs enable gate D (zone C4) HIGH which is applied through jumper JE/JF to pin 9 of NAND gate K (zone B4). During an output instruction, the $\overline{SOUT}$ and PWR signals (zone B6) are generated by the CPU which enables NAND gate K (zone B4) output LOW. The LOW is applied through jumper JD/JC and inverted HIGH by gate J (zone C3) and presented to the STB input (zone B4) of latch G.

The data from the CPU is presented to the Interface (sheet 1, zone C1) and stored in data latch G (sheet 3, zone B4) during the output instruction because the STB and MD inputs are enabled.

The outputs of data latch G light the appropriate data LED (DØ-D7) on the Display/Control Panel (Figure 3-16, sheet 3, zone D2). After the machine cycle is complete, NAND gate Z (sheet 1, zone B7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit binary counter to address 066_8.

The data (013_8) in address location 066_8 is stored in data latch A (zone D8) and enables the S5, S7, and S8 outputs (zone D7) HIGH. After the completion of this operation, NAND gate Z is enabled, and the 4-bit binary counter is incremented to address 067_8. Address 067_8 contains a jump instruction (303_8) which is stored in the CPU in the same manner as the previous instructions. The jump instruction will force the CPU back to the original P counter address which was stored in data latches B1 and T (zone B5) at the beginning of the ACC display operation. The remainder of the ACC display operation will transfer the address stored (AØ-A7) in B1 and (A8-A15) in T to the CPU. After the jump instruction is stored in the CPU, the 4-bit binary counter is incremented to address 070_8.

The data in address location 070_8 is present on the RDØ through RD7 outputs (043_8) and applied to data latch A (zone D8). The data present at latch A is stored by the A output of the 4-bit binary counter (zone B9) being LOW during even addresses and the generation of the CS strobe (C6, C7, and $\overline{C8}$ HIGH). The 043_8 data enables outputs S3, S7, and S8 (zone D7) HIGH. Output S3 is applied to the DS2 input of data latch B1 (zone C5), presenting the output data (AØ-A7) to the Interface as $\overline{FDIØ}$ through $\overline{FDI7}$. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gate J (zone D6) and are used to generate the $\overline{SB}$ and $\overline{FDIG2}$ signals as described in the previous instruction transfers. With the data present to the Interface and the associated circuits conditioned, NAND gate Z (zone A7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 071_8.

The data in address 071_8 is not stored in latch A because it is an odd address. However, the A output (zone B9) is applied to pins 1 and 5 of NAND gates J (zone D6) as a HIGH, enabling the CS signal to produce the $\overline{SB}$ and $\overline{FDIG2}$ outputs. The $\overline{SB}$ and $\overline{FDIG2}$ signals allow the transfer of the first eight address data latch

bits to the CPU, and the operation is identical to the previous instructions.

After the CPU receives the eight address bits, the 4-bit binary counter increments to address 072_8. The data in 072_8 (023_8) is stored in latch A (zone D7) because it is an even address. The 023_8 data enables S4, S7, and S8 (zone D7) HIGH. Output S4 is applied to the DS2 input of data latch T (zone A6), presenting the output data (A8-A15) to the Interface as $\overline{FDI\emptyset}$ through $\overline{FDI7}$. Outputs S7 and S8 condition NAND gates J (zone D6) and are used to generate $\overline{SB}$ and $\overline{FDIG2}$ during the next address (073_8). With the data present to the Interface and the associated circuits conditioned, NAND gate Z (zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 073_8.

Address 073_8 operation is the same as address 071_8, allowing the A8 through A15 address data to be stored in the CPU. Address 074_8 clears the data latch A (zone D7) and allows the CPU to jump to the original P counter address, conditioning the CPU for normal operation.

After conditioning the CPU, the 4-bit binary counter (zone A9) is incremented to address 075_8. The data in 075_8 (177_8) is applied to NAND gate N (zone B7), producing a HIGH at gate Z (zone B8). The HIGH at gate Z disables NAND gate Z (zone A8), inhibiting any following clock pulses to the 4-bit binary counter, thus ending the ACC display operation.

3-39. 8800b OPTIONS

The 8800b has several options which may be selected by the operator. Two options may be used on the Display/Control card, and three options may be used on the Interface card.

3-40. DISPLAY/CONTROL CARD OPTIONS

The Display/Control card options contain a choice of front panel slow operation clock frequencies and a choice of completing one instruction cycle or machine cycle in single step or slow operation. The normal slow operation clock frequency requires a

connection between jumpers JA and JD (Figure 3-16, sheet 1, zone D2). For slower operation, jumpers JB to JD or JC to JD may be connected. The normal single/step or slow operation requires a connection between jumpers JE and JF (sheet 2, zone D7) which allows the 8800b CPU to complete one instruction cycle before resuming a wait condition. However, if the operator wishes to execute one machine cycle after each single/step or slow operation, remove jumpers JE and JF which disables the $\overline{DO5}$ signal (zone D8).

3-41. INTERFACE CARD OPTIONS

One Interface Card option allows the operator to monitor any data from an external device on the DØ through D7 front panel LEDs. Data may be monitored from an external device if jumpers JA and JB are connected (Figure 3-15, sheet 3, zone C3). NAND gate K is enabled LOW when the Ø1, $\overline{PDBIN}$, and $\overline{SINP}$ signals (zone C6) are present during an external device to CPU data transfer. The LOW is presented through JB and JA (zone C3) to gate J which produces a HIGH to the STB input of data latch G (zone B4). The HIGH on STB allows the data present on the DOØ-DO7 line (zone B6) to be displayed on the DØ-D7 LEDs on the front panel.

The remaining Interface card options pertain to jumpers JE and JF (zone C4) and jumpers JD and JC (zone C3). If jumpers JE and JF and JC and JD are connected, only data addressed to the front panel (377_8) is displayed. If jumpers JE and JF are removed, all output data from the CPU is displayed on the front panel.

3-42. 8800b POWER SUPPLIES

The 8800b requires a positive 8 volt, 18 ampere supply, a positive 18 volt, 2 ampere supply, and a -18 volt, 2 ampere supply (Figure 3-17). When the ON/OFF switch on the front panel is positioned to ON, a 110 AC voltage is applied to transformer T1. Two bridge rectifiers on the secondary of T1 produce the positive 8, 18, and negative 18 voltage supplies which are applied to the 8800b circuits. The positive and negative 18 volt supplies are pre-regulated by the Q1 and Q2 transistor circuits on the power supply board.

The 8800b printed circuit cards receive the supply voltages on the bus. Each printed circuit card contains its own voltage regulator circuits which produce the operating voltage for the particular printed circuit card.

The CPU card (Figure 3-18) requires a regulated positive and negative 5 volt source and a regulated positive 12 volt source. These voltages are produced by VR1, VR2, and D2 circuits.

The Interface card (Figure 3-19) requires a regulated positive 5 volt source which is produced by the VR1 circuit.

The Display/Control card (Figure 3-20) requires an unregulated positive 8 volt source, a regulated positive 5 volt source, and a regulated negative 9 volt source. The regulated voltages are produced by the VR1 and VR2 circuits.

Table 3-3. Bus Definitions

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	+8v	+8 volts	Unregulated voltage on bus, supplied to PC boards and regulated to 5v.
2	+18v	+18 volts	Positive pre-regulated voltage.
3	XRDY	EXTERNAL READY	External ready input to CPU board's ready circuitry
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt Line #7	
12	*XRDY2	EXTERNAL READY #2	A second external ready line similar to XRDY
13 to 17	To be defined		
18	$\overline{\text{STAT DSB}}$	$\overline{\text{STATUS DISABLE}}$	Allows the buffers for the 8 status lines to be tri-stated
19	$\overline{\text{C/C DSB}}$	$\overline{\text{COMMAND/CONTROL DISABLE}}$	Allows the buffers for the 6 output command/ control lines to be tri-stated
20	UNPROT	UNPROTECT	Input to the memory protect flip-flop on a given memory board

*New bus signal for 8800b.

PIN NUMBER	SYMBOL	NAME	FUNCTION
21	55	SINGLE STEP	Indicates that the machine is in the process of performing a single step (i.e. that SS flip-flop on D/C is set)
22	$\overline{\text{ADD DSB}}$	$\overline{\text{ADDRESS DISABLE}}$	Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DBS}}$	$\overline{\text{DATA OUT DISABLE}}$	Allows the buffers for the 8 data output lines to be tri-stated
24	Ø2	PHASE 2 CLOCK	
25	Ø1	PHASE 1 CLOCK	
26	PHLDA	HOLD ACKNOWLEDGE	Processor command/control output signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle
27	PWAIT	WAIT	Processor command/control signal that appears in response to the READY signal going low; indicates processor will enter a series of .5 microsecond WAIT states until READY again goes high.
28	PINTE	INTERRUPT ENABLE	Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are inhibited.
29	A5	Address Line #5	
30	A4	Address Line #4	

PIN NUMBER	SYMBOL	NAME	FUNCTION
31	A3	Address Line #3	
32	A15	Address Line #15	(MSB)
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DO1	Data Out Line #1	
36	DO0	Data Out Line #0	(LSB)
37	A10	Address Line #10	
38	DO4	Data Out Line #4	
39	DO5	Data Out Line #5	
40	DO6	Data Out Line #6	
41	DI2	Data In Line #2	
42	DI3	Data In Line #3	
43	DI7	Data In Line #7	(MSB)
44	SM1	MACHINE CYCLE 1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUTPUT	Status output signal that indicates the address bus contains the address of an output device and the data bus will contain the output data when $\overline{PWR}$ is active
46	SINP	INPUT	Status output signal that indicates the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMORY READ	Status output signal that indicates the data bus will be used to read memory data
48	SHLTA	HALT	Status output signal that acknowledges a HALT instruction
49	$\overline{CLOCK}$	$\overline{CLOCK}$	Inverted output of the Ø2 CLOCK

PIN NUMBER	SYMBOL	NAME	FUNCTION
50	GND	GROUND	
51	+8v	+8 volts	Unregulated input to 5 volt regulators
52	-18v	-18 volts	Negative pre-regulated voltage
53	$\overline{\text{SSWI}}$	$\overline{\text{SENSE SWITCH INPUT}}$	Indicates that an input data transfer from the sense switches is to take place. This signal is used by the Display/ Control logic to: a) Enable sense switch drivers b) Enable the Display/ Control board drivers Data Input (FDIØ-FDI7) c) Disable the CPU board Data Input Drivers (DIØ-DI7)
54	$\overline{\text{EXT CLR}}$	$\overline{\text{EXTERNAL CLEAR}}$	Clear signal for I/O devices (front panel switch closure to ground)
55	*RTC	REAL TIME CLOCK	60Hz signal used as timing reference by the Real Time Clock/Vectored Interrupt Board
56	*$\overline{\text{STSTB}}$	$\overline{\text{STATUS STROBE}}$	Output strobe signal supplied by the 8224 clock generator. Primary purpose is to strobe the 8212 status latch so that status is set up as soon in the machine cycle as possible. This signal is also used by Display/Control logic.
57	*DIG1	DATA INPUT GATE #1	Output signal from the Display/Control logic that determines which set of Data Input Drivers have control of the CPU board's bidirectional data bus. If DIG1 is HIGH, the CPU drivers have control; if it is LOW the Display/ Control logic drivers have control.

*New bus signal for 8800b.

PIN NUMBER	SYMBOL	NAME	FUNCTION
58	*FRDY	FRONT PANEL READY	Output signal from D/C logic that allows the front panel to control the READY line to the CPU
59 to 67	TO BE DEFINED		
68	MWRITE	MEMORY WRITE	Indicates that the data present on the Data Out Bus is to be written into the memory location currently on the address bus
69	$\overline{PS}$	$\overline{PROTECT\ STATUS}$	Indicates the status of the memory protect flip-flop on the memory board currently addressed
70	PROT	PROTECT	Input to the memory protect flip-flop on the memory board currently addressed
71	RUN	RUN	Indicates that the STOP/RUN flip-flop is Reset; i.e. machine is in RUN mode
72	PRDY	PROCESSOR READY	Memory and I/O input to the CPU board wait circuitry
73	$\overline{PINT}$	$\overline{INTERRUPT\ REQUEST}$	The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request.
74	$\overline{PHOLD}$	$\overline{HOLD}$	Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle

*New bus signal for 8800b.

PIN NUMBER	SYMBOL	NAME	FUNCTION
75	$\overline{\text{PRESET}}$	$\overline{\text{RESET}}$	Processor command/control input; while activated, the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	Processor command/control output; provides a signal to indicate the beginning of each machine cycle
77	$\overline{\text{PWR}}$	$\overline{\text{WRITE}}$	Processor command/control output; used for memory write or I/O output control. Data on the data bus is stable while the $\overline{\text{PWR}}$ is active
78	PDBIN	DATA BUS IN	Processor command/control output; indicates to external circuits that the data bus is in the input mode
79	A0	Address Line #0	(LSB)
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DO2	Data Out Line #2	
89	DO3	Data Out Line #3	
90	DO7	Data Out Line #7	
91	DI4	Data In Line #4	
92	DI5	Data In Line #5	
93	DI6	Data In Line #6	
94	DI1	Data In Line #1	
95	DI0	Data In Line #0	(LSB)
96	SINTA	INTERRUPT ACKNOWLEDGE	Status output signal; acknowledges signal for INTERRUPT request

PIN NUMBER	SYMBOL	NAME	FUNCTION
97	$\overline{SWO}$	$\overline{WRITE\ OUT}$	Status output signal; indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer
99	$\overline{POC}$	$\overline{POWER\text{-}ON\ CLEAR}$	
100	GND	GROUND	

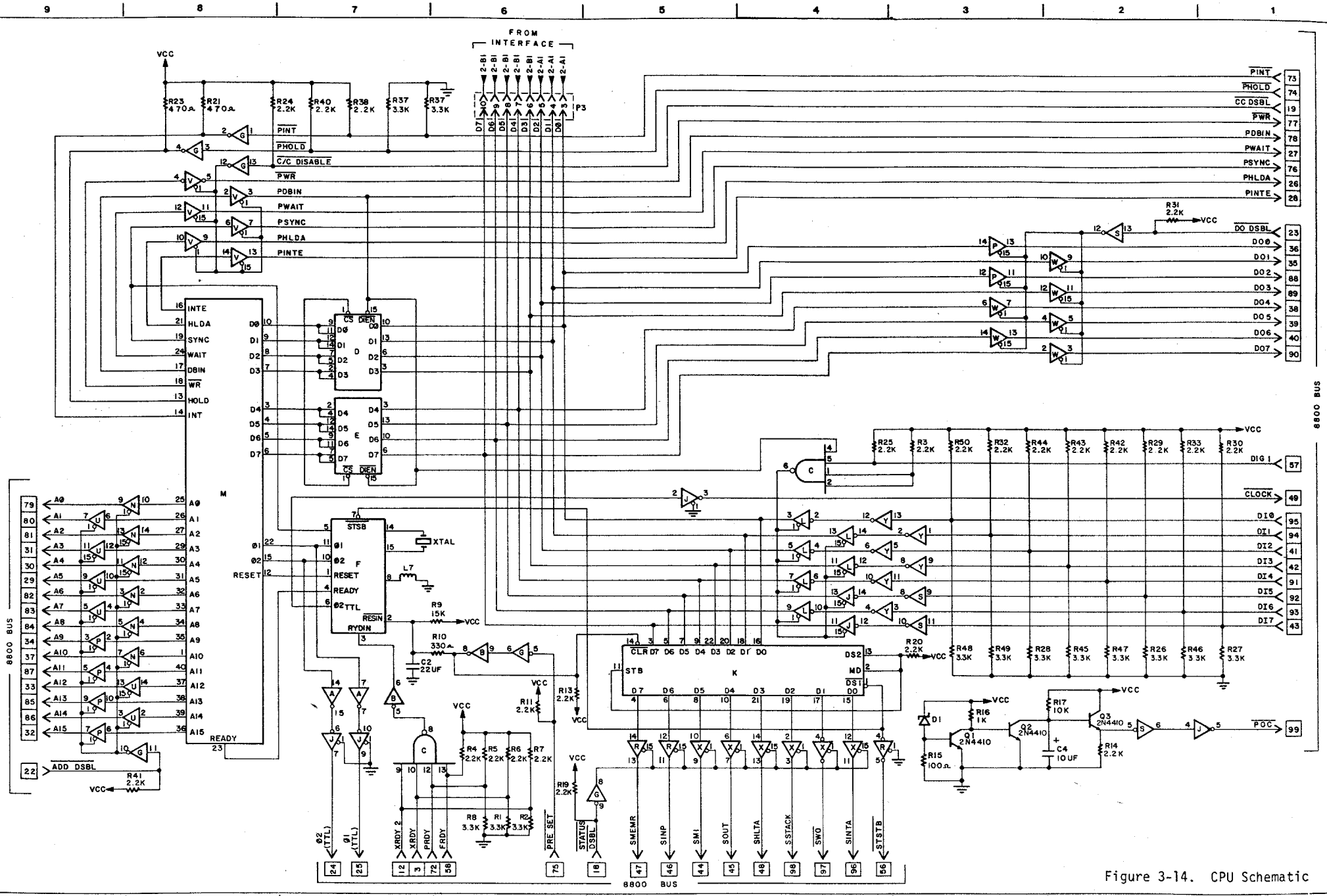


Figure 3-14. CPU Schematic

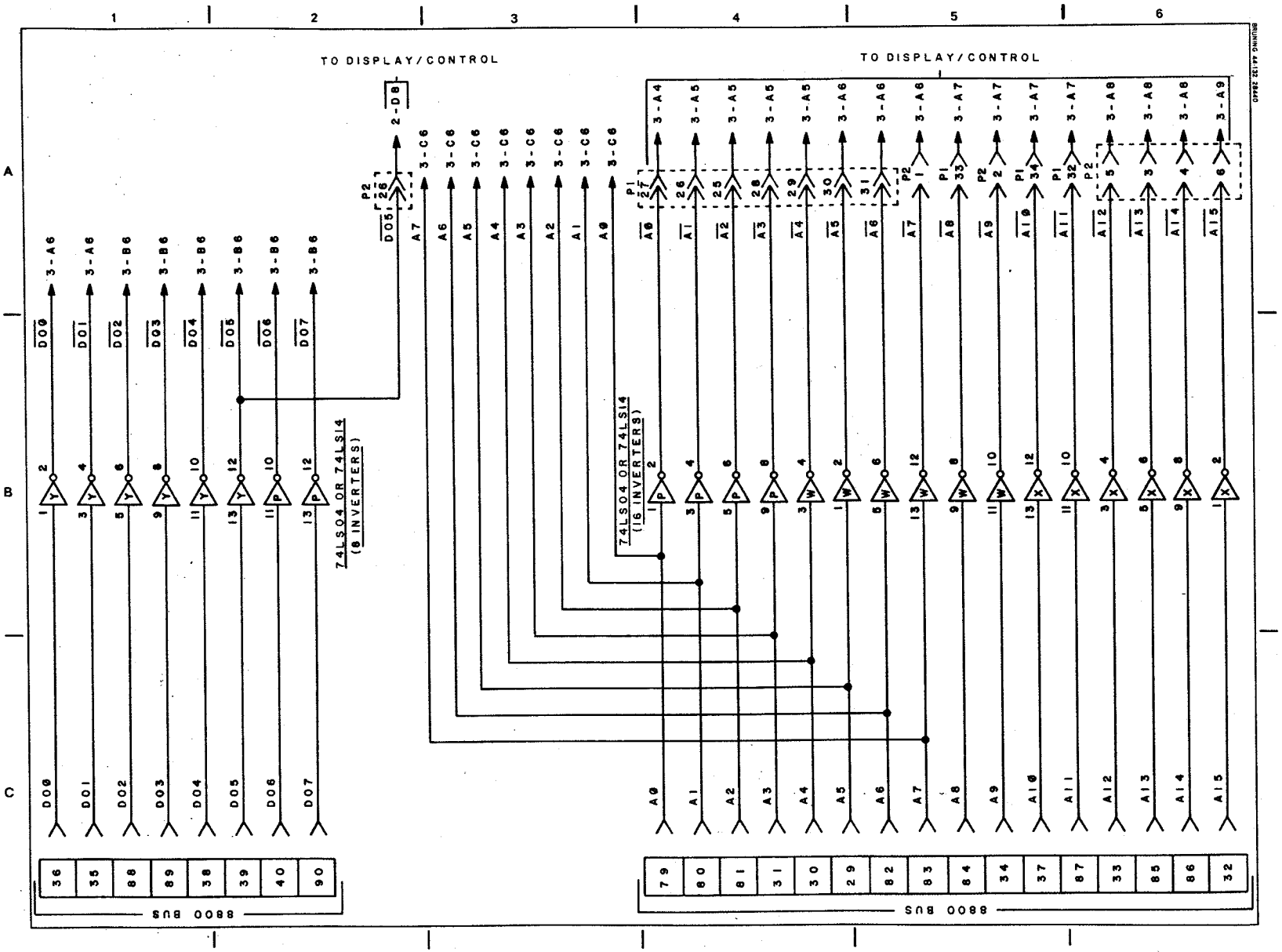


Figure 3-15. Interface Schematic (sheet 1 of 3)

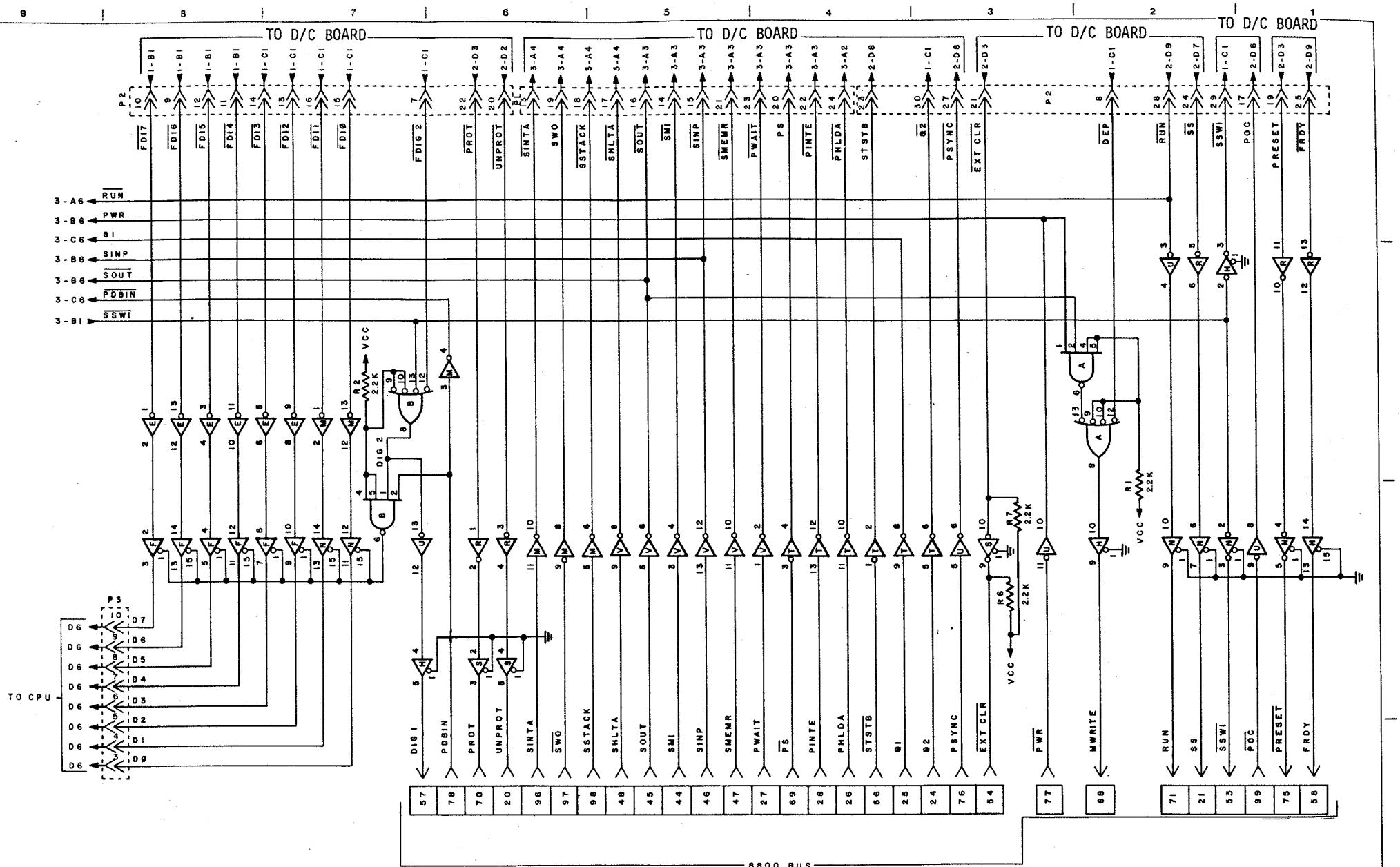


Figure 3-15. Interface Schematic (sheet 2 of 3)

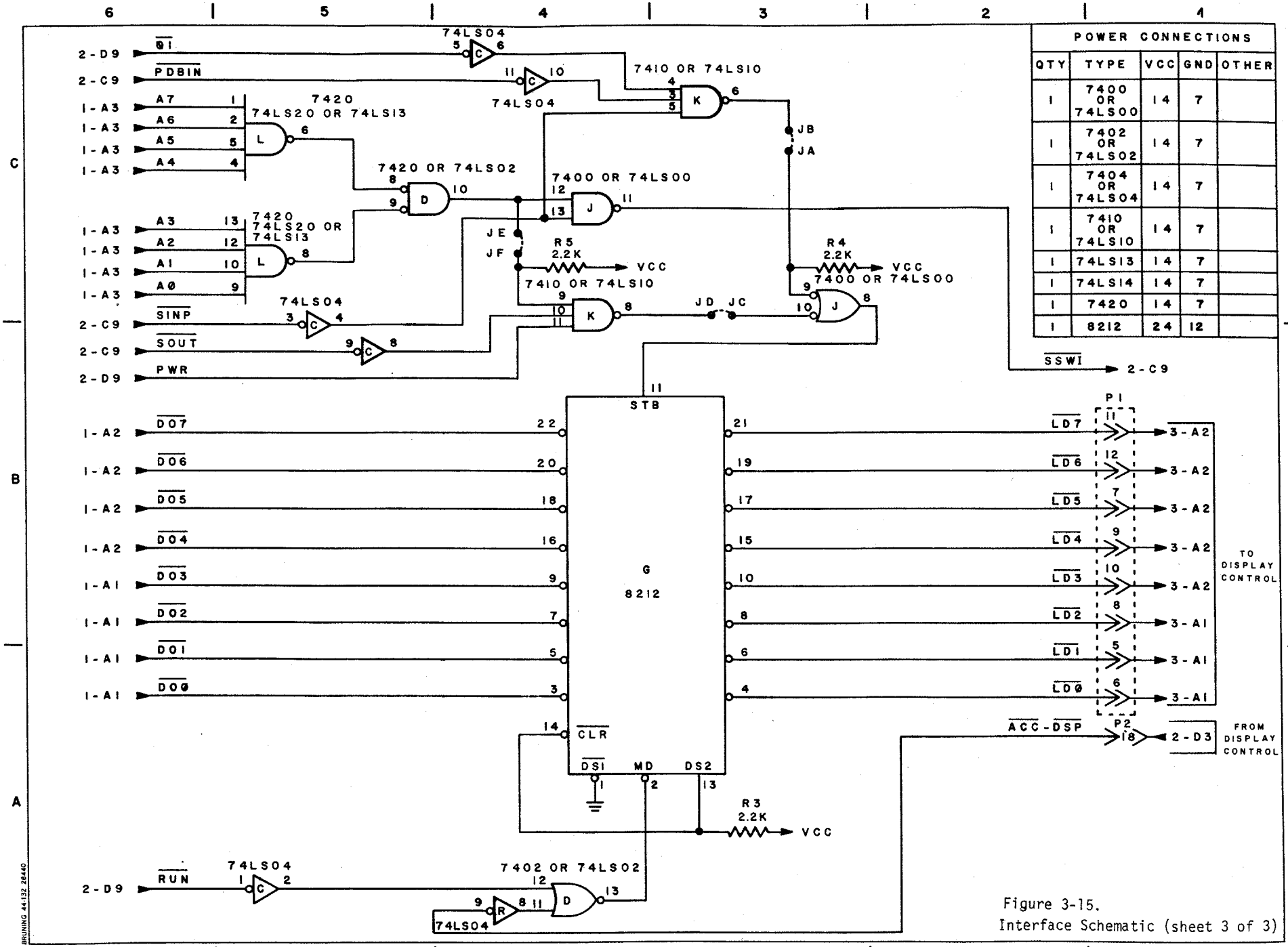
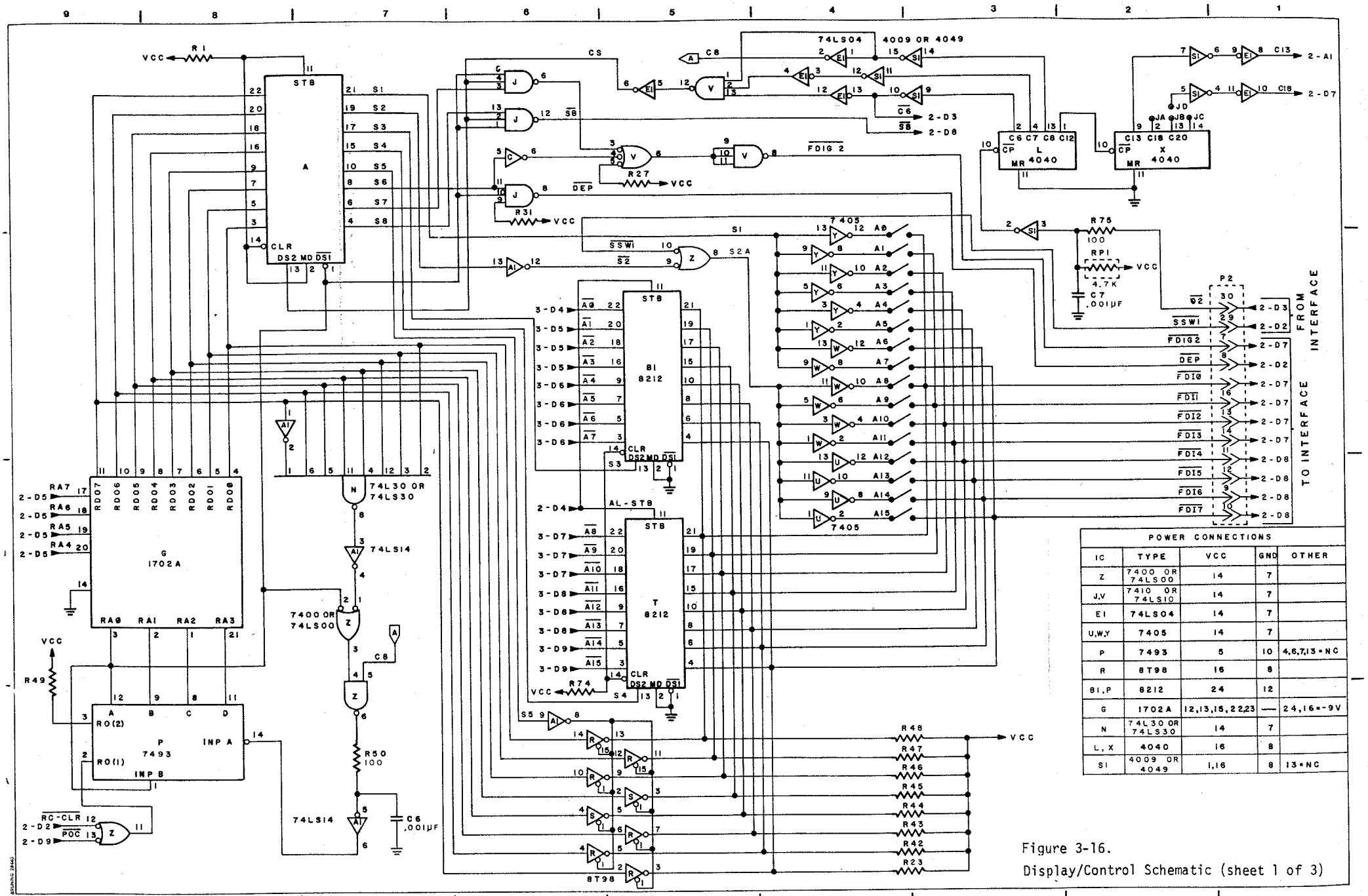


Figure 3-15.
Interface Schematic (sheet 3 of 3)



POWER CONNECTIONS				
IC	TYPE	VCC	GND	OTHER
Z	7400 OR 74LS00	14	7	
J,V	7410 OR 74LS10	14	7	
E1	74LS04	14	7	
U,W,Y	7405	14	7	
P	7493	5	10	4,6,7,13=NC
R	8T98	16	8	
B1,P	8212	24	12	
G	1702A	12,13,15,22,23	—	24,16=-9V
N	74L30 OR 74LS30	14	7	
L, X	4040	16	8	
S1	4009 OR 4049	1,16	8	13=NC

Figure 3-16.
Display/Control Schematic (sheet 1 of 3)

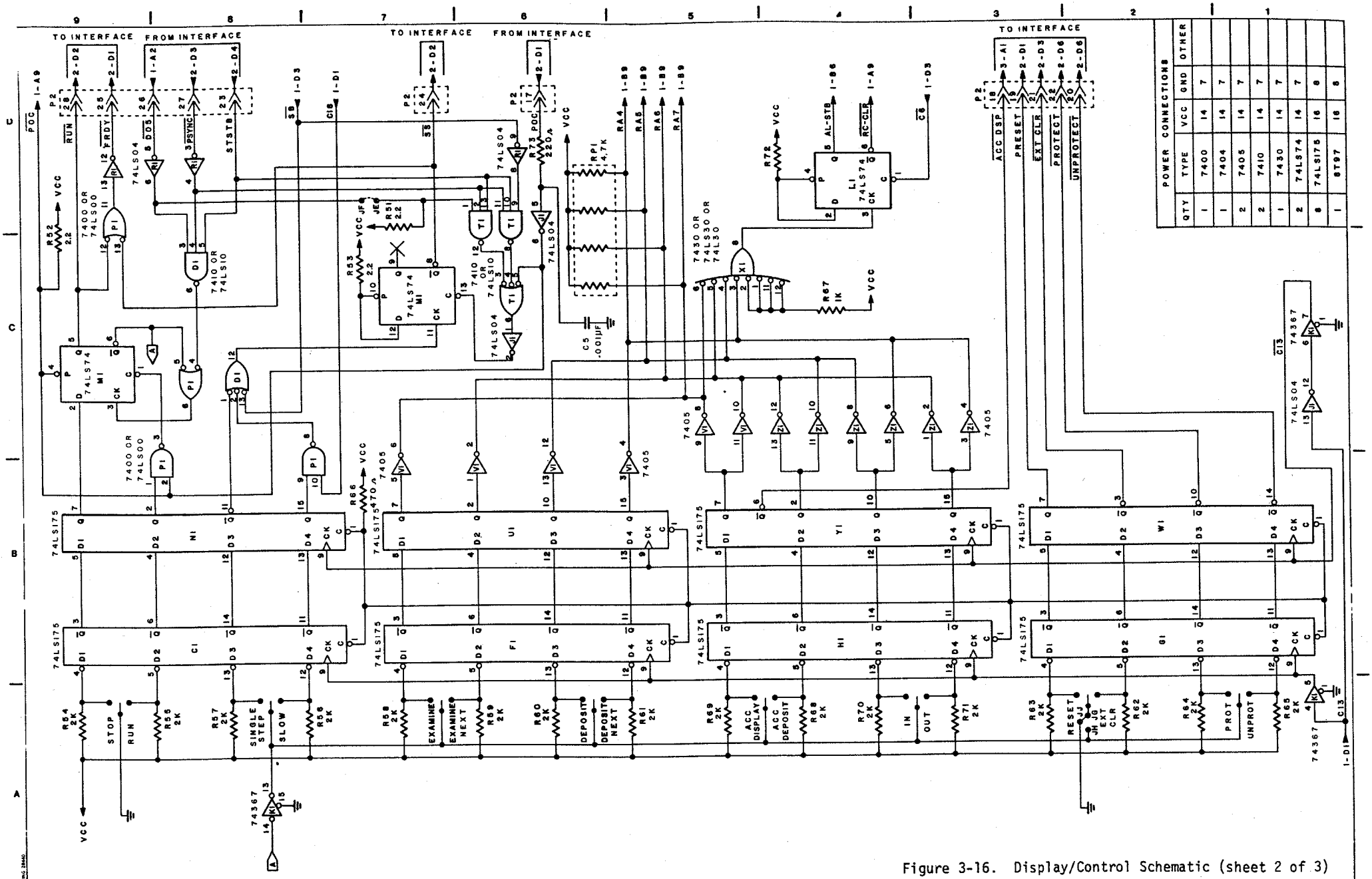
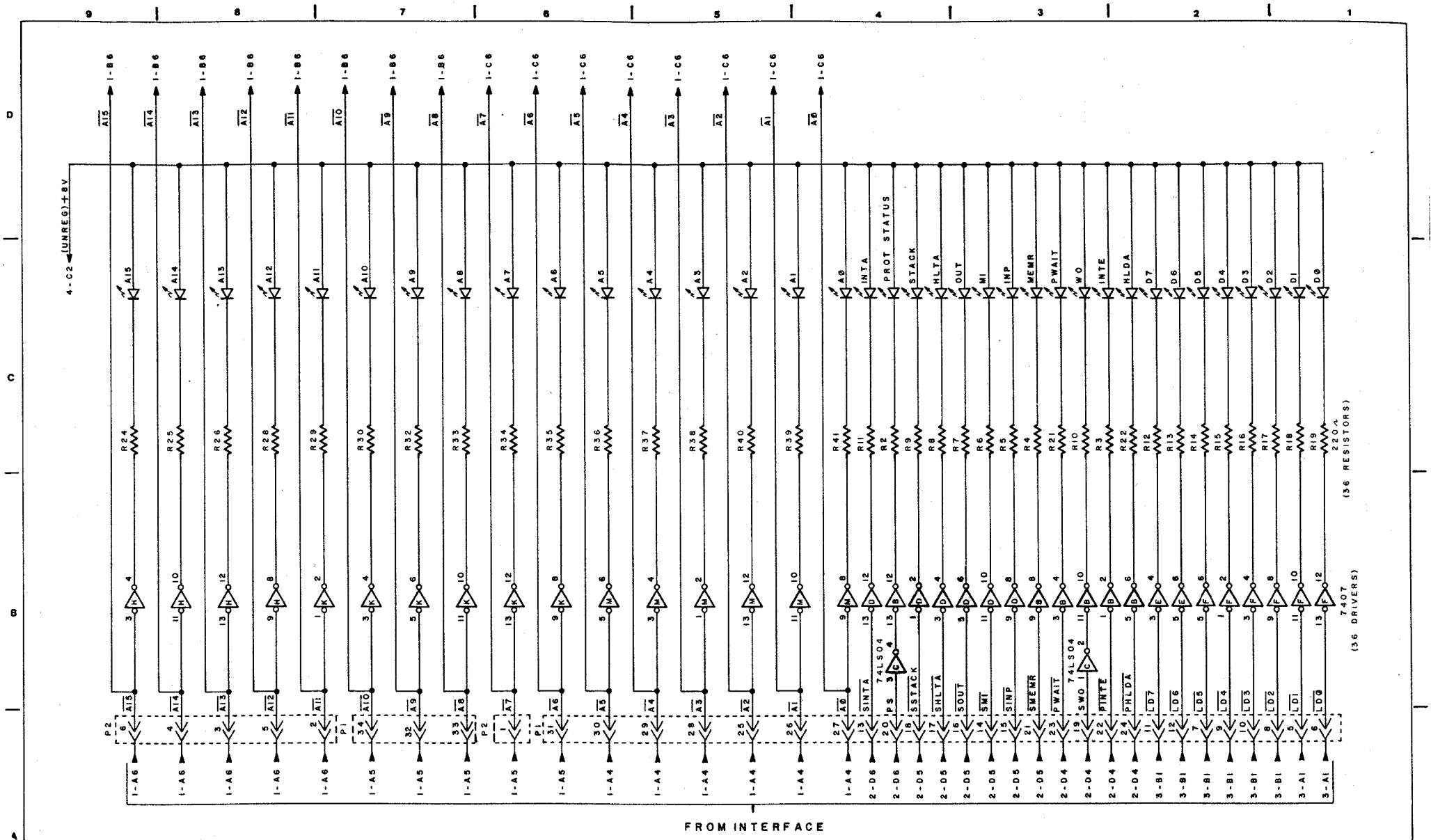
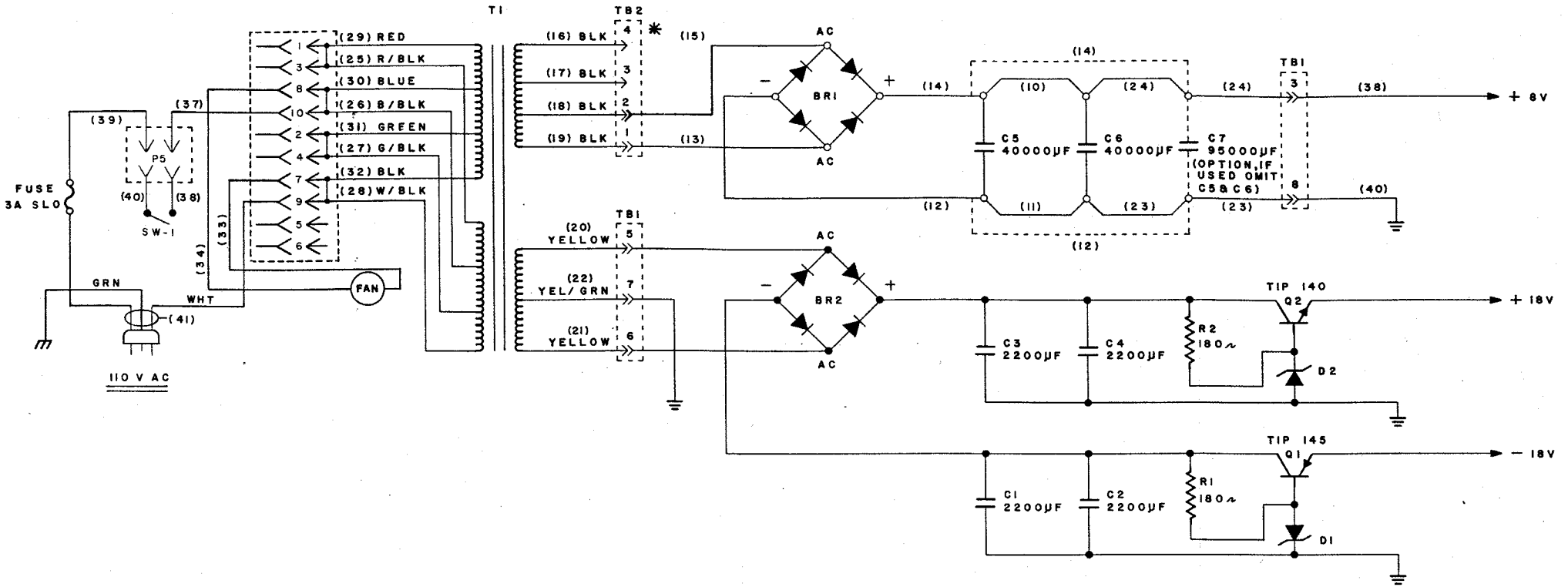


Figure 3-16. Display/Control Schematic (sheet 2 of 3)



POWER CONNECTIONS				
QTY	TYPE	VCC	GND	OTHER
7	7407	14	7	
1	74LS04	14	7	

Figure 3-16. Display/Control Schematic (sheet 3 of 3)



90 V
// GREEN & GRN./BLK. TO PIN 1
// BLACK & WHT./BLK. TO PIN 2

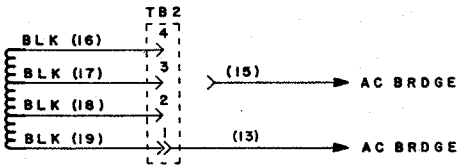
110 V
// BLUE & BLUE/BLK. TO PIN 1
// BLACK & WHT./BLK. TO PIN 2

130 V
// RED & RED/BLK. TO PIN 1
// BLACK & WHT./BLK. TO PIN 2

180 V
IN 1 WHT./BLK.
IN 2 GREEN
JUMP
BLACK & GREEN/BLK.

220 V
IN 1 WHT./BLK.
IN 2 BLUE
JUMP
BLACK & BLUE/BLK.

260 V
IN 1 WHT./BLK.
IN 2 RED
JUMP
BLACK & RED/BLACK

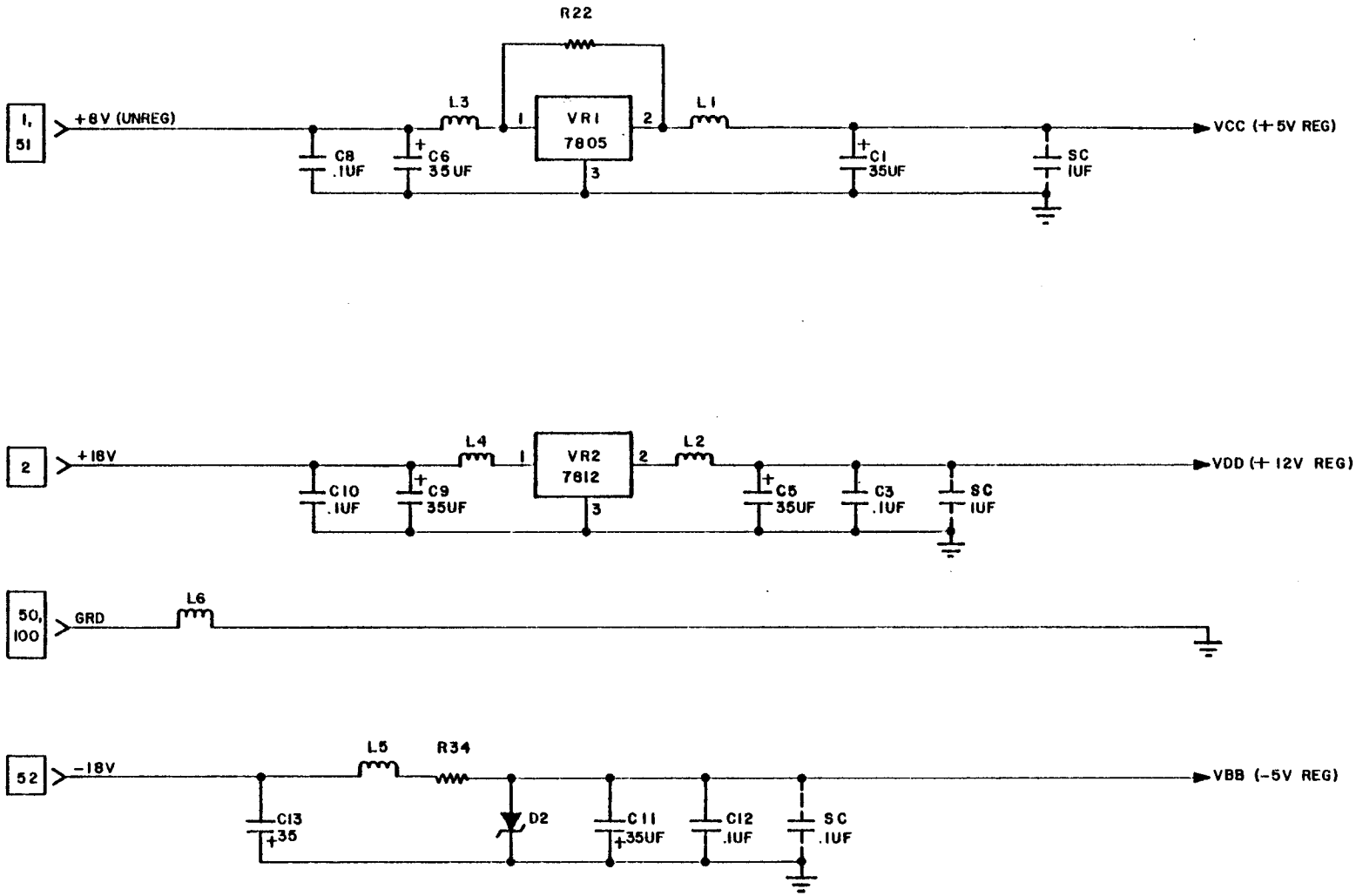


*

AMPS	TB2
0 - 4	pin 2
4 - 9	pin 3
9 - 18	pin 4

8800b

Figure 3-17. Power Supply Board Schematic



REF DESIG	TYPE	VCC	GRD	OTHER	REF DESIG	TYPE	VCC	GRD	OTHER
					M	8080A	20	2	
G, B	74LS04	14	7		J, X, R, V, N, U, P	74368 OR 8T98	16	8	
C	74LS13 OR 74LS20	14	7		K	8212	24	12	
S, Y	74LS14	14	7		D, E	8216	16	8	
					F	8224	16	8	VDD = 9
P, W	74367	16	8		A	4009	1	8	VDD = 16

Figure 3-18. CPU Voltage Regulator Schematic

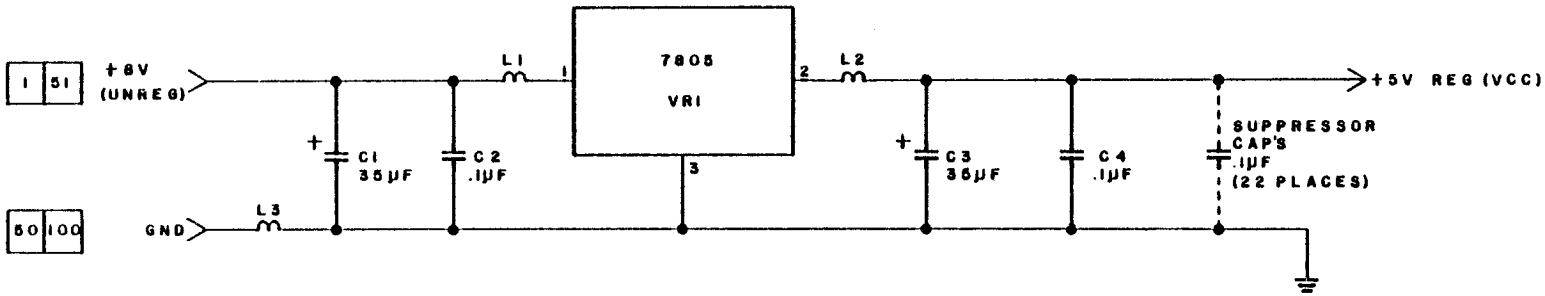


Figure 3-19. Interface Voltage Regulator Schematic

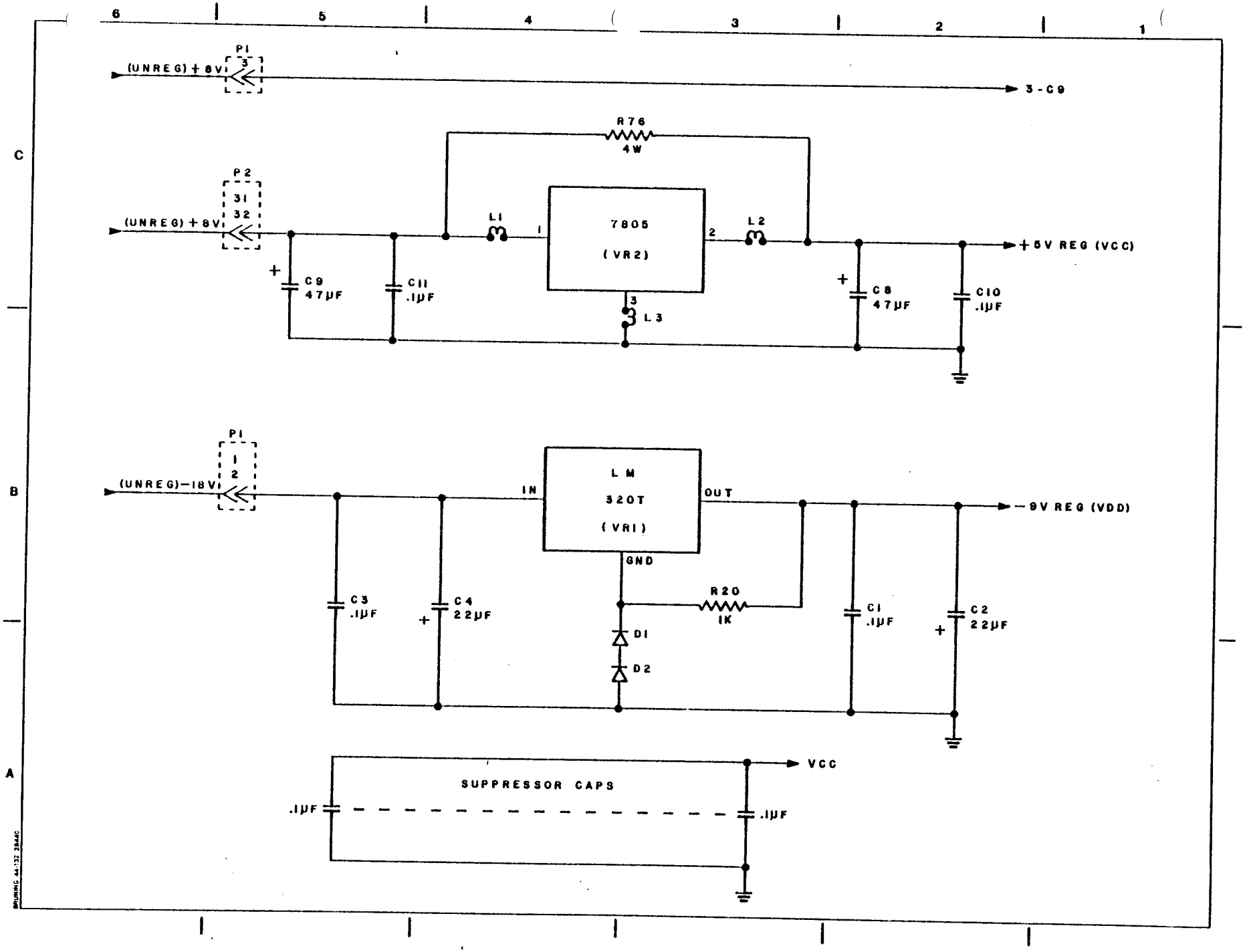


Figure 3-20. Display/Control Voltage Regulator Schematic