Step	Instructions	If Correct	If Incorrect
B.	Incorrect installation of Interface cables P1 and P2 can cause damage to several components. Refer to page 5-19 to check for improper cable assembly and repair if necessary. Then follow the steps below:	If P1 and P2 were correctly installed, proceed to Step C.	
	1) Check ICs H, K, B1 and T on the Display/Control board according to the instructions on page 4-5.		Replace as necessary.
	2) Turn power off and unsolder one lead of R74 on the Display/Control board. Test for a resistance reading of 2.2K ohms. Resolder the lead to the board.		Replace as necessary.
	3) Turn power on and check the +5v voltage regulator and the -9v voltage regulator on the Display/Control board as described on page 4-18, step 1.		Repair according to the instructions on page 4-18.

Step	Instructions	If Correct	If Incorrect
	C. Electrical Problem.		
	1) With the computer in a Run state, check for irregular HIGH pulses at IC M1 pin 3 on the Display/Control board.	If pulses are present, proceed to Step 2) on page 4-38.	If pulses are not present, check the logic from IC M1 to IC D1 on the Display/Control board. HIGH pulses should be present at pins 3, 4 and 5 of IC D1. a. If pulses are missing from pin 3 (of IC D1), check pin 4 of IC M on the CPU board for positive pulses. If absent, check ICs M and F according to the instructions on page 4-20, Step 6. If pulses are present at IC M pin 4, check IC E pin 1 on the CPU board for a constant LOW signal. If absent, check continuity from pin 1 to Ground. Check pin 15 (of IC E) for a LOW PDBIN pulse. If pin 15 is HIGH, check IC V on the CPU board according to the instructions on page 4-5. If IC V is working properly, check pin 17 of IC M for LOW pulses. If absent, again check ICs M and F according to the instructions on page 4-20, step 6. Check pin 13 of IC E for a HIGH DO5 signal. If present, trace continuity and logic to IC D1 on the Display/Control board. Repair as necessary. b. If the PSYNC pulse is missing at pin 4 of IC D1, check for a HIGH pulse at pin 19 of IC M on the CPU board. If absent, check ICs F and M according to the instructions on page 4-5,

Step	Instructions	If Correct	If Incorrect
			step 6. If the HIGH pulse is present at pin 19, check continuity and logic from pin 19 to pin 4 of IC D1. Check ICs, if necessary, according to the instructions on page 4-5.
			c. If the HIGH pulse (STSTB) is absent at pin 5 of IC D1 on the Display/Control board, check for a LOW pulse at pin 7 of IC F on the CPU board. If absent, check for a HIGH PSYNC signal at pin 5 of IC F. If absent, trace continuity to IC M pin 19. If continuity is present, check ICs F and M according to the instructions on page 4-20, step 6. If the LOW pulse is present at pin 7 of IC F, trace logic and continuity to pin 5 of IC D1 on the Display/Control board, and repair as necessary.
	2) Lift the STOP switch and check pin 4 of IC C1, pin 5 of IC N1 and pin 2 of IC M1 on the Display/Control board.	C1 pin 4 should be LOW. N1 pin 5 should be HIGH. M1 pin 2 should be HIGH. Proceed to Step 3).	Pin 1 of ICs C1 and N1 should be HIGH. If not, trace continuity to Vcc, and repair as necessary. Check ICs C1, N1 and M1 according to the instructions on page 4-5. (Note: M1 pin 2 is HIGH only when the STOP switch is lifted and held.)
	3) Lift the STOP switch and check pins 4, 1 and 5 of IC M1.	Pins 4 and 1 should be HIGH; pin 5 should be HIGH. Proceed to Step 3 on page 4-39.	If pin 4 is LOW, check $\overline{POC}$ according to the instructions on page 4-22, step 11. If pin 1 of IC M1 is LOW, check IC P1 according to the instructions on page 4-5. Pin 1 of IC P1 should be LOW when the STOP switch is pressed. If not, check logic at pins 2 and 4 of IC N1 and at pins 5 and 6 of IC C1. If pin 5 of IC M1 is LOW, check pin

Step	Instructions	If Correct	If Incorrect
			2 for a HIGH. If absent, check the logic of ICs C1 and N1. If pin 2 is HIGH, check IC M1 according to the instructions on page 4-5.
3	SS Circuitry.		
	A. (Note: If the JE to JF jumper is present on the Display/Control board, it should be removed for this check.) Check for LOW going clear pulses on IC M1 pin 13 on the Display/Control board while the chassis is in a Run state. A LOW at IC T1 pin 8 on the Display/Control board should produce the LOW clearing pulse at IC M1 pin 13.	If clear pulses are present on IC M, the trouble lies in the $\overline{SB}$ circuitry. Proceed to Step B.	If pulses are absent at M1 pin 13, check for proper logic at ICs J1 and T1 on the Display/Control board. If the PSYNC and/or STSTB signals are absent at the inputs of IC T1, refer to Step C on page 4-37.
	B. If LOW $\overline{SB}$ pulses are present, follow the steps below:		
	1) Check pin 2 of IC J on the Display/Control board for a CS waveform (see waveform #5 on page 4-30).	If present, proceed to Step 2).	If absent, refer to Section 4-3, Step 13, page 4-23.
	2) Check pin 13 of IC J for a constant LOW level.	If absent, check pin 13 of IC A for a CS signal. If the signal is absent	If a constant HIGH level is present at IC J pin 13, check continuity to pin 4 of IC A. Check IC A according to the instructions on page 4-5.

Step	Instructions	If Correct	If Incorrect
		at IC A, refer to Section 4-3, Step 13, page 4-23.	
	3) Check pins 2, 11 and 14 of IC A on the Display/Control board for HIGH signals.	If present, proceed to Step 4).	If absent, trace continuity to VR1 pin 2 and repair as necessary.
	4) Trace continuity from pin 1 of IC J to pin 1 of IC A and to pins 12 and 1 of IC P.	If continuity is present, proceed to Step C.	Repair as necessary.
C.	Check pin 14 of IC P on the Display/Control board for a C8 signal.	If present, proceed to Step D.	If absent, refer to Section 4-3, Step 15, page 4-24. Check the logic operation of IC Z.
D.	Check for a HIGH at IC P pin 3 on the Display/Control board.	If present, proceed to Step E.	If absent, trace continuity through R49 to VR1 pin 2 (on the Display/Control board). Repair as necessary.
E.	Check pin 2 of IC P for a LOW level. Pin 2 should pulse HIGH only when a PROM related switch is pressed.	If present, proceed to Step F.	If absent, check for HIGH $\overline{\text{RC-CLR}}$ and $\overline{\text{POC}}$ levels at pins 12 and 13 of IC Z. If $\overline{\text{POC}}$ is LOW, refer to Section 4-3, Step 7, page 4-20. A LOW signal at $\overline{\text{RC-CLR}}$ indicates either no $\overline{\text{C6}}$ signal at IC L1 pin 1 on the Display/Control board (refer to Section 4-3, Step 14, page 4-24) or LOW going pulses on pin 3 of IC L1. LOW pulses at IC L1 pin 3 should occur only when a PROM related switch is pressed. Check for HIGHs at IC L1 pins 2 and 4. If absent, trace continuity to VR1 pin 2 and

Step	Instructions	If Correct	If Incorrect
			repair as necessary.
F.	A C8 signal at IC P pin 14 should cause HIGH going pulses to appear at pins 8, 9, 11 and 12 of IC P (RA0-RA13) on the Display/Control board. (Note: The C8 signal will occur only briefly when a PROM related switch is pressed.)	If HIGH pulses are present, proceed to Step G.	If HIGH pulses are not present, check continuity from pin 1 to pin 12 of IC P. Check power and Ground at IC P. If present, turn power off and remove IC G. Turn power on and check again for pulses at pins 8, 9, 11 or 12. If absent, check IC P according to the instructions on page 4-5. Turn power off and reinstall IC G.
G.	Check pins 17, 18, 19 and 20 of IC G on the Display/Control board for HIGHs. (LOWs should occur only when the appropriate PROM related switches are pressed.)	If present, proceed to Step H.	If any LOW levels are present (but no PROM related switches are pressed), trace logic through ICs V1, Z1, U1, F1, Y1 and H1. Pin 1 of ICs F1, U1, H1 and Y1 should be LOW. If not, trace continuity to Vcc. Check and replace ICs if necessary.
H.	Check pins 1, 2, 3, 4, 5, 6, 11 and 12 of IC N on the Display/Control board for pulses.	If present, proceed to Step I.	If constant levels rather than pulses are present, refer to Section 4-3, step 16 on page 4-24. Also check for shorts and bad socket connections.
I.	Check IC A1 pins 1 and 2 on the Display/Control board for proper inverting logic.	If IC A1 is working properly, proceed to Step J.	If proper inverting logic is not present, check IC A1 according to the instructions on page 4-5.
J.	On the Display/Control board, compare the signal at IC A pin 1 to that of IC P pin 12.	If the signals match, proceed to Step K.	If the signals do not match, trace continuity to Vcc and repair as necessary.

Step	Instructions	If Correct	If Incorrect
K.	Check for pulses at pins 3 and 4 of IC A.	If present, proceed to Step L.	If pulses are absent at pin 3, trace continuity to pin 4 of IC G and repair as necessary. If the pulse is absent at pin 4 of IC A, turn power off and remove pin 4 from the board. Trace logic to pin 12 of IC J. If the pulse is present while pin 4 is removed from the board, trace continuity and look for shorts. If the pulse is absent while pin 4 is removed from the board, turn power off and replace IC A with either IC B1 or IC T. If pulses are now present at pins 3 and 4, IC A is defective and should be replaced.
L.	Check for a LOW at IC N pin 8 and trace logic to pin 4 of IC Z on the Display/ Control board. A LOW at Z pin 4 should prevent the C8 signal from appearing at pin 6 of IC Z and pin 14 of IC P and should keep IC P from incrementing. (Note: Pin 4 of IC Z should be LOW when the computer is stopped. Pin 4 should pulse HIGH only when a PROM related switch is pressed.)	If a LOW is present at pin 8 of IC N and if proper logic is present, proceed to Table 4-6.	Check any ICs that do not follow their respective truth tables according to the instructions on page 4-5. Check for continuity and shorts from pin 12 of IC P to pin 2 of IC Z and repair as necessary.

Table 4-6. Run Check

Problem

Description: When the computer is running, the WAIT light on the front panel should be dim or off, and a HIGH should be present at pin 23 of IC M on the CPU board. If the computer will not run when the RUN switch is pressed, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Press and hold the RUN switch and check for LOWs at ICs C1 pin 5 and M1 pin 2 on the Display/Control board. Check for HIGHs at ICs N1 pin 4 and P1 pin 1 (on the Display/Control board).	If present, proceed to Step 2.	If absent, trace logic to the RUN/STOP switch. Check ICs C1 and N1 according to the instructions on page 4-5.
2	The HIGH at pin 1 of IC P1 should produce a LOW at pin 1 of IC M1, causing a LOW at pin 5. A LOW at M1 pin 5 should produce a LOW at IC R1 pin 12. Trace this active LOW $\overline{\text{FRDY}}$ level through the Interface board to IC C pin 13 on the CPU board. (IC C pin 13 should be HIGH when the RUN switch is pressed.) The resulting HIGH at pin 3 of IC F should cause a HIGH at pin 23 of IC M (on the CPU board).	If proper logic operation is present, proceed to Table 4-7.	If a LOW is not present at pin 5 of IC M1, check the logic of IC P1 and, if necessary, check the ICs according to the instructions on page 4-5. Check for Ø2, Vcc and Ground at IC F. If IC F or IC M appears defective, refer to Section 4-3, Step 6, page 4-20.

Table 4-7. Single Step/Slow Check

Problem

Description: If JE is jumpered to JF on the Display/Control board, SINGLE STEP/SLOW can be misleading. For example, when SINGLE STEP/SLOW is pressed for a JMP, a change cannot be detected in the LEDs. Activity can only be detected by monitoring pulses on IC M pin 23 (READY) on the CPU board. If pulses are not present at IC M, a problem exists in the SINGLE STEP/SLOW circuitry. Follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	If SINGLE STEP will not function, follow steps A and B below:		
	A. While pressing the SINGLE STEP switch, check for LOWs at ICs C1 pin 13 and D1 pin 1 on the Display/Control board.	If present, proceed to Step B.	If absent, check for HIGH signals at pin 1 of ICs C1 and N1 on the Display/Control board. If absent, trace continuity to VR1 pin 2. If the HIGH signal is present, check ICs C1 and N1 according to the instructions on page 4-5. If IC D1 pin 2 is LOW, check pin 15 of IC N1 for a LOW. If absent, check pin 9 of ICs C1 and N1 for a $\overline{C13}$ waveform. If the waveform is absent, refer to Section 4-3, Step 13, page 4-23. If pin 15 is HIGH, recheck the logic of ICs N1 and C1. Pin 13 of IC N1 should be HIGH. If not, trace continuity from pin 13 of IC D1 to pin 12 of IC J and repair as necessary.
	B. When the SINGLE STEP switch is pressed and held, IC M1 pin 11 on the Display/Control board should go HIGH. Check	If HIGH signals and proper logic are present, proceed to Step 2.	Check IC D1 according to the instructions on page 4-5. Check the logic from pin 8 of IC M1 on the Display/Control board to pin 23 of IC M on the CPU board. Check any suspected ICs according to

Step	Instructions	If Correct	If Incorrect
	for HIGHs at pins 12, 10 and 13 of IC M1. (Note: A constant HIGH should be present at pin 13. A LOW pulse, however, will end the SINGLE STEP operation.) Trace the LOW pulse at IC M1 pin 8 to a HIGH pulse at pin 23 of IC M on the CPU board.		the instructions on page 4-5. If problems are suspected with IC F or IC M, refer to page 4-20, step 6.
2	If SLOW (on the Display/Control board) will not function, follow steps A, B and C below:		
	A. Check for C18 pulses at pin 10 of IC P1 on the Display/Control board.	If present, proceed to Step B.	If absent, check the logic from pin 10 of IC P1 to jumper JD. (JD is located next to switch A1.) If pulses are not present at pins 2, 13 and 14 of IC X, refer to Section 4-3, steps 9 and 10 on page 4-22 to check ICs L and X.
	B. Holding the SLOW switch down should produce HIGHs at pin 9 of IC P1 and at pins 1 and 13 of IC D1 on the Display/Control board.	If present, proceed to Step C.	If pin 13 of IC D1 is LOW, check IC J pins 1, 2 and 13 as described in Table 4-5, Step 3, page 4-39. If pin 9 of IC P1 or pin 1 of IC D1 is LOW, check the logic of ICs C1 and N1. Check ICs C1 and N1 according to the instructions on page 4-5 if necessary.
	C. C18 pulses should occur at ICs D1 pin 2 and M1 pin 11 on the Display/Control	If proper operation is present, proceed to Step 3.	If LOW pulses are absent at pin 13 of IC M1, refer to step A on page 4-39. Any IC whose logic does not follow its truth table should be

Step	Instructions	If Correct	If Incorrect
	board. LOW going pulses should be present at IC M1 pin 13. (Note: A constant LOW level should never be present at M1 pin 13.) Pins 12 and 10 of IC M should be HIGH. Trace the LOW going pulses at IC M1 pin 8 to the HIGH going pulses on the READY line (pin 23 of IC M on the CPU board).		checked according to the instructions on page 4-5. HIGH pulses should be present at pin 3 of IC F on the CPU board. If ICs M or F appear defective, refer to Section 4-3, steps 5 and 6, page 4-20.
3	If SINGLE STEP and SLOW will not actuate a stopped condition, follow steps A and B below:		
	A. Pressing the SINGLE STEP/ SLOW switch should produce LOWs at ICs M1 pin 2 and P1 pin 1 and HIGHs at ICs M1 pin 1 and P1 pin 12 on the Display/Control board. Check for a LOW going pulse at pin 13 of IC M1. (Note: This pulse may be hard to detect. If so, hit the RUN switch to produce several of these pulses	If the proper signals are present, proceed to Step B.	Check any IC whose logic does not follow its truth table according to the instructions on page 4-5. Pin 1 of ICs C1 and N1 should be HIGH. If not, trace continuity to VR1 pin 2 and repair as necessary. If pin 13 of IC M1 is constantly LOW, refer to Step A, page 4-39.

Step	Instructions	If Correct	If Incorrect
	B. Check pin 5 of IC T1 on the Display/Control board for a HIGH $\overline{POC}$ signal. HIGH going pulses should be present at pins 3 and 4 of IC T1.	If present, proceed to Table 4-8.	If a HIGH $\overline{POC}$ signal is not present at pin 5, refer to Section 4-3, step 11, page 4-22. If HIGH going pulses are absent at pins 3 and 4, check for PSYNC and STSTB pulses at pins 2, 13, 11 and 10 of IC T1. If these pulses are missing, trace logic to the CPU board according to the instructions on page 4-37, step C. Check any suspected ICs according to the instructions on page 4-5.

Table 4-8. Protect/Unprotect Check

Note 1: Table 4-8 deals with problems on the Display/Control board only; memory board problems are not included in this table.

Note 2: In order to perform the PROTECT/UNPROTECT check, one memory board that has the PROTECT/UNPROTECT option must be installed in the chassis. (16K Static boards do not have this function. PROM memory boards, when addressed, always cause the PROTECT LED to light.)

Problem Description: If pressing the PROTECT switch does not protect the memory board from depositing new data and if the UNPROTECT switch does not allow new data to be deposited, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Pressing the PROTECT (or UNPROTECT) should produce a LOW at pin 13 of IC G1 on the Display/Control board as long as the switch is held. Pressing the UNPROTECT switch causes the same operation to occur at pin 12 of IC G1. The LOW at pin 13 of IC G1 causes a LOW at pin 10 of IC W1 (for PROTECT). The LOW at pin 12 of IC G1 causes a LOW at pin 14 of IC W1 (for UNPROTECT). Trace the LOW active $\overline{\text{PROTECT}}$ (or UNPROTECT) signal to bus pin 20 (or 70). (Note: The memory board must be addressed in order to be protected.)	If proper operation is present, proceed to Step 2.	Check ICs G1 and W1 according to the instructions on page 4-5. Check any IC (on the Interface board) whose logic does not follow its truth table according to the instructions on page 4-5.

Step	Instructions	If Correct	If Incorrect
2	A LOW on the PS line (bus #69) should cause the PROTECT LED to light.	If so, proceed to Table 4-9 on page 4-50.	If the PROTECT LED does not light, refer to Section 4-3, step 17 on page 4-24.

Table 4-9. Sense Switch Check

Problem

Description: If the data input from the SENSE switches does not match the settings of A8-A15, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Pressing Single Step twice for the following program should produce LOW levels at pins 8 and 9 of IC D on the Interface board. (Note: JE should not be jumpered to JF on the Display/Control board for this check.) All address lines (AØ-A15) should be HIGH. Location / Bit Pattern 000 333 001 377 002 303 003 000 004 000 Note: If this program cannot be deposited, proceed to Table 11 on page 4-55 to correct the DEPOSIT problem.	If LOWs are present at pins 8 and 9 when the program is run, proceed to Step 2.	If LOW levels are not present at pins 8 and 9 of IC D, check the logic operation from IC M (AØ-A15) on the CPU board to IC D on the Interface board. Check any suspected ICs according to the instructions on page 4-5.
2	Pin 12 of IC J on the Interface board should be HIGH.	If so, proceed to Step 3.	If pin 12 is LOW, check IC D according to the instructions on page 4-5.
3	Pin 13 of IC J should be HIGH. If not, check for a HIGH SINP signal at bus pin 46.	If pin 13 of IC J is HIGH, proceed to Step 4.	If pin 13 of IC J is not HIGH, check IC C according to the instructions on page 4-5. If the SINP signal is absent at bus pin 46, trace logic to pin 6 of IC K on the CPU board. Check

Step	Instructions	If Correct	If Incorrect
			any suspected ICs according to the instructions on page 4-5. Check for HIGHs at pins 2, 11 and 13 of IC K. If absent, trace continuity to VR1 pin 2 on the CPU board, and repair as necessary. Press RUN and check for LOW $\overline{\text{STSTB}}$ pulses on pin 1 of IC K (see Table 4-10, Step 3 on page 4-53).
4	Pin 11 of IC J on the Interface board ($\overline{\text{SSWI}}$) should be LOW. Checking logic and continuity, trace this signal to a LOW on pin 10 of IC Z on the Display/ Control board.	If correct, proceed to Step 5.	Check the logic of ICs J and H on the Interface board. Check any suspected ICs according to the instructions on page 4-5.
5	For each address switch (A8-A15) that is lifted, the corresponding output pin of either IC W or IC U on the Display/Control board should be LOW.	If LOWs are present at the proper IC pins, proceed to Step 6.	If these IC pins are HIGH, check for shorts. Check ICs W and U according to the instructions on page 4-5.
6	Trace the LOW level output from IC W or IC U to a HIGH on the corresponding output pin of IC E or IC M on the Interface board.	If proper logic is present, proceed to Step 7.	Check any suspected ICs according to the instructions on page 4-5.
7	Check PDBIN (pin 2 of IC B on the Interface board and pin 4 of IC C on the CPU board) for HIGH levels.	If present, proceed to Step 8.	If absent, check IC V on the CPU board according to the instructions on page 4-5. Trace logic to a HIGH at pin 17 of IC M on the CPU board. Check any suspected ICs according to the instructions

Step	Instructions	If Correct	If Incorrect
			on page 4-5.
8	A LOW $\overline{\text{SSWI}}$ level should produce LOWs at pins 6 and 13 of IC B on the Interface board. Pin 8 of IC B should be HIGH, causing LOWs to appear at bus pin 57 (DIG1) and pin 6 of IC B. A LOW at pin 57 should produce a HIGH at pin 6 of IC C on the CPU board. Pins 4, 5, 9 and 10 of IC B should be HIGH.	If correct, proceed to Step 9.	If any of these signals are incorrect or absent, check continuity and check the ICs according to the instructions on page 4-5. If HIGHs are not present at IC B pins 4, 5, 9 and 10, trace continuity to VR1 pin 2 on the Interface board.
9	Refer to schematic 3-14. Lifting any of the A8-A15 address switches should cause the corresponding data line of ICs D, E and M on the CPU board to go HIGH.	If the proper data lines are HIGH, proceed to Table 4-10.	Check logic from the outputs of ICs E and M on the Interface board to ICs D and E on the CPU board. Check any suspected ICs according to the instructions on page 4-5.

Table 4-10. Status Check

Problem

Description: If status is incorrect when the computer is turned on and if pressing the RESET switch fails to achieve proper status, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Check for HIGHs at pins 2, 13, 11 and 14 of IC K on the CPU board.	If present, proceed to Step 2.	If pins 2, 13, 11 or 14 are LOW, trace continuity to VR1 pin 2 on the CPU board. Repair as necessary.
2	$\overline{\text{PRESET}}$ should be HIGH on the bus.	If so, proceed to Step 3.	If not, check the logic for the RESET switch according to the instructions in Table 4, page 4-32.
3	Check for a LOW going $\overline{\text{STSTB}}$ pulse at pin 1 of IC K on the CPU board while the computer is running.	If present, proceed to Step 4.	If absent, check continuity from pin 7 of IC F to pin 1 of IC K. If continuity is absent, check IC F on the CPU board according to the instructions in Table 5, Step C, page 4-38.
4	Check for MEMR and M1 signals at IC K pins 4 and 8 on the CPU board. Check continuity from the outputs of ICs D and E to the inputs of IC K on the CPU board.	If present, proceed to Step 5.	If pins 3 and 7 of IC K are constantly LOW when the computer is running, look for shorts on the CPU board and repair as necessary.
5	If pins 4 and 8 of IC K are HIGH, the M1 and MEMR LEDs on the front panel should be lit.	If the correct LEDs are lit, proceed to Section 4-5 if problems exist with the EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, ACCUMULATOR DISPLAY/ ACCUMULATOR LOAD or IN/ OUT switches.	If the correct LEDs are not lit, check for proper logic operation from IC K on the CPU board to the front panel LEDs. Check any suspected ICs according to the instructions on page 4-5. If the ICs are working properly, refer to Step 17 on page 4-24 to check the LED circuitry.

4-5. PROM RELATED SWITCH PROBLEMS

Section 4-5 contains procedures to solve problems relating to the EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, ACCUMULATOR DISPLAY/ACCUMULATOR LOAD and IN/OUT switches. Problems involving the RESET, RUN/STOP, SINGLE STEP/SLOW, PROTECT/UNPROTECT, SENSE and STATUS switches should be checked before performing the tests in Section 4-5. Refer to Section 4-4 to solve problems of this type.

The text in Section 4-5 is divided into 16 major steps. These are general procedures that should always be followed when testing the PROM related switches.

Table 4-11. PROM Related Switch Problems

Step	Instructions	If Correct	If Incorrect
1	When a PROM related switch is pressed and held, the upper four bits (RA7-RA4) of the beginning address (as shown in Table 3-2 in the Theory of Operation section) are produced on the PROM (IC G on the Display/Control board) address lines. The chart below shows how the PROM address lines (RA7-RA4) correspond to the switch.	If RA7-RA4 go to the appropriate levels when the corresponding switch is pressed, proceed to Step 2.	If RA7-RA4 are LOW when none of the switches are pressed, check for LOW input signals at ICs V1 and Z1 on the Display/Control board. Trace continuity from RA4-RA7 through RP1 to VR1 pin 2 (Vcc), and repair as necessary. If a HIGH input is found, check the logic operation of ICs F1, U1, A1 and V1. Pin 1 of ICs H1, U1, Y1 and F1 should be HIGH. If not, trace to VR1 pin 2 on the Display/Control board. Pins 4, 5, 13 and 12 of ICs F1 and H1 should be HIGH when none of the switches are pressed. If HIGH signals are not present, trace continuity to VR1 pin 2 and repair as necessary. Press and hold down the suspected switch and trace logic to the switch from pins 17, 18, 19 and 20 of IC G on the Display/Control board. Check any suspected ICs according to the instructions on page 4-5.

Address Bit

	RA7	RA6	RA5	RA4
Corresponding PROM Pin	17	18	19	20
Switch				
EXAMINE	LOW	HIGH	HIGH	HIGH
EXAMINE NEXT	HIGH	LOW	HIGH	HIGH
DEPOSIT	HIGH	HIGH	LOW	HIGH
DEPOSIT NEXT	HIGH	HIGH	HIGH	LOW
ACCUMULATOR DISPLAY	LOW	LOW	HIGH	HIGH
ACCUMULATOR LOAD	HIGH	LOW	LOW	HIGH
IN	HIGH	HIGH	LOW	LOW
OUT	HIGH	LOW	HIGH	LOW

If no PROM related switches are pressed, RA7-RA4 (pins 17-20 of IC G) should be HIGH.

Step	Instructions	If Correct	If Incorrect
2	Check for a HIGH clear pulse (less than .1 μsec. wide) at pin 2 of IC P on the Display/Control board each time a PROM related switch is pressed. (Note: In order to better detect this pulse, turn the scope's time base to the lowest frequency setting, or highest time/cm setting, and turn up the intensity. A logic probe may also be needed.)	If the pulse is present, proceed to Step 3.	If the pulse is absent, check for HIGHs at pins 2 and 4 of IC L and at pins 1, 2, 11 and 12 of IC X1 on the Display/Control board. If absent, trace continuity to VR1 pin 2 on the Display/Control board. Repair as necessary. Pressing any PROM related switch will cause at least one LOW on the input pins of IC X1, producing a HIGH at pin 3 of IC L1. The LOW going pulse at pin 6 ($\overline{RC}$-$\overline{CLR}$) of IC L1 should cause a HIGH pulse at pin 2 of IC P. At the same time, pin 5 (AL-STB) of IC L1 should pulse HIGH. If this does not occur, check ICs L1 and Z according to the instructions on page 4-5.
3	Refer to schematic 3-16, sheet 1 of 3. Press the PROM related switch and check for proper operation (as shown in schematic 3-16) on the RAØ-RA3 address lines of IC G on the Display/Control board. For example, the DEPOSIT switch covers addresses 320-323. Address lines RA2 and RA3 (which correspond to pins 8 and 11, respectively, of IC P) are never used. Consequently, when the DEPOSIT switch is pressed,	If address lines RAØ-RA3 are operating properly, proceed to Step 4.	If proper operation is not present at address lines RAØ-RA3, check IC P according to the instructions in Table 4-5, Step F, on page 4-41.

Step	Instructions	If Correct	If Incorrect

pulses should not be present at pins 8 and 11 of IC P. When the switch is released, pulses may be present at all outputs of IC P. The following chart shows the correct pulse level for each switch.

Switch	Address Bit			
	RA3	RA2	RA1	RA0
EXAMINE	NP	P	P	P
EXAMINE NEXT	NP	NP	P	P
DEPOSIT	NP	NP	P	P
DEPOSIT NEXT	NP	P	P	P
ACCUMULATOR DISPLAY	P	P	P	P
ACCUMULATOR LOAD	P	P	P	P
IN	P	P	P	P
OUT	P	P	P	P

NP = No pulses

P = Pulses

(Note: This chart is valid only when the switch is pressed and held. When the switch is released, pulses may appear at all of the address lines.)

Step	Instructions	If Correct	If Incorrect
4	For each data line, check continuity (with an ohmmeter set at X1K or higher) from the output pins of ICs N and F on the Interface board to the appropriate pins of ICs D and E on the CPU board.	If continuity is present, proceed to Step 5.	If continuity is absent, check for opens or a bad connection in the CPU to Interface board cable. An open will cause the same bit to be deposited no matter what condition the AØ-A7 switches are in. The EXAMINE switch will show that the address bit is HIGH along with the corresponding bit in addresses A8-A15. Resolder the cable if necessary and solder over opens.
5	If a pulse counter is available, check for the appropriate number of clock pulses at IC M1 pin 11 on the Display/Control board as listed below:	If correct, proceed to Step 6.	If the correct number of pulses is not present at IC M1 pin 11, check IC G on the Display/Control board. Also check CS, C8, $\overline{C13}$, C6 and M1 (refer to pages 4-23 step 13, 4-24 step 15, 4-22 step 10, 4-24 step 14 and 4-37 step C, respectively).

Switch	Number of Pulses
EXAMINE	3
EXAMINE NEXT	1
DEPOSIT	0
DEPOSIT NEXT	1
ACCUMULATOR DISPLAY	6
ACCUMULATOR LOAD	6
INPUT	6
OUTPUT	6

(Note: Each number corresponds to the number of S8 pulses set in Table 3-2.)

Step	Instructions	If Correct	If Incorrect
6	If the $\overline{C13}$, $\overline{C6}$, C8 and CS signals have not been checked, refer to page 4-22 step 10, page 4-24 step 14, page 4-24 step 15, and page 4-23 step 13, respectively, to check these signals.	If these signals are functioning properly, proceed to Step 7.	Repair according to the instructions on the appropriate page.
7	The PROM functions usually cause each PROM data output to change levels at least once. Bit 7 of EXAMINE NEXT is the only exception to this rule. Press each PROM related switch while monitoring the output pins of IC G on the Display/Control board for pulses.	If constant levels are not present, proceed to Step 8.	If a constant LOW or HIGH signal is present on pins 4, 5, 6, 7, 8, 9, 10 or 11 of IC G on the Display/Control board when a switch is pressed, check continuity with an ohmmeter and look for shorts and bad socket connections. Repair as necessary.
8	Check for HIGH signals at pins 2, 14 and 11 of IC A on the Display/Control board. Check continuity from pins 1 and 12 of IC P to pin 1 of IC A and to pin 2 of IC Z on the Display/Control board.	If HIGH signals and continuity are present, proceed to Step 9.	If HIGH signals and/or continuity are absent, check continuity from the suspected pin to VR1 pin 2 on the Display/Control board and repair as necessary.
9	One second after the switch is pressed, the final address (as shown in Table 3-2) should appear on lines RA0-RA7 and remain there until the switch	If correct, proceed to Step 10.	If the final address is not 177, check IC G according to the instructions on page 4-24, step 16. Also look for shorts and repair as necessary.

Step	Instructions	If Correct	If Incorrect
	is released. 177 should also be present at IC G on the Display/ Control board.		
10	Refer to the following chart and check for S pulses at pins 4, 6, 8, 10, 15, 17, 19 or 21 of IC A on the Display/Control board.	If present, proceed to Step 11.	If the proper pulses are absent, or if the improper pulses are present at IC A, check IC A according to the instructions on page 4-5. Also look for shorts and repair as necessary.
	Switch — S Pulse EXAMINE — S1, S2, S5, S7, S8 EXAMINE NEXT — S5, S7, S8 DEPOSIT — S1, S6, S7 DEPOSIT NEXT — S1, S6, S7, S8, S5 ACCUMULATOR DISPLAY — S3, S4, S5, S7, S8 ACCUMULATOR LOAD — S1, S3, S4, S5, S7 S8 IN — S2, S3, S4, S5, S7, S8 OUT — S2, S3, S4, S5, S7, S8		
11	The S pulses listed in Step 10 should produce the following results:		
	A. For each AØ-A7 switch that is up, S1 should produce a HIGH pulse on the corresponding output pin of IC E	If present, proceed to Step B.	If these HIGH pulses are absent, trace continuity from pin 21 of IC A to the input pins of ICs Y and W on the Display/Control board. Also trace continuity from the output pins of ICs Y and W

Step	Instructions	If Correct	If Incorrect
	or IC M on the Interface board. To check for S1, press the DEPOSIT switch.		to the input pins of ICs E and M on the Interface board with the corresponding switch up. Repair as necessary. Check logic operation from the input pins of ICs Y and W on the Display/Control board to the output pins of ICs E and M on the Interface board. Check any suspected ICs according to the instructions on page 4-5.
B.	A HIGH S2 pulse should cause LOW pulses at the outputs of ICs W and U on the Display/Control board (if the corresponding switch is up).	If LOW pulses are present, proceed to Step C.	If LOW pulses are absent, check the logic of ICs A1, Z, W and V. Test the ICs according to the instructions on page 4-5, if necessary.
C.	HIGH S3 and S4 pulses should produce HIGHs at ICs B1 pin 13 and T pin 13 on the Display/Control board.	If HIGH signals are present at B1 pin 13 and T pin 13, proceed to Step D.	If HIGH pulses are absent, check continuity with an ohmmeter and repair as necessary.
D.	A HIGH S5 pulse should produce LOWs at IC R pins 1 and 15 and IC S pin 1 on the Display/Control board.	If LOW signals are present, proceed to Step E.	If LOW signals are absent, check continuity from pin 10 of IC A to pin 9 of IC A1 on the Display/Control board. If the logic on IC A1 is incorrect, check the IC according to the instructions on page 4-5.
E.	A HIGH S6 pulse should produce a HIGH MWRITE pulse at bus pin 68 and a HIGH DIG1 pulse at bus pin 57.	If HIGH pulses are present, proceed to Step F.	If a HIGH MWRITE pulse is absent at bus pin 68, check for a LOW $\overline{\text{DEP}}$ pulse at pin 8 of IC J. If absent, check pin 10 of IC J on the Display/

Step	Instructions	If Correct	If Incorrect
	If the MWRITE signal is absent, "1's" will appear in the data lights (for each AØ-A7 switch that is up) for as long as the DEPOSIT switch is held. When the DEPOSIT switch is released, the data lights will return to their original pattern. The DEPOSIT NEXT switch will act as EXAMINE NEXT, i.e. it will increment an address, but fail to deposit it in memory.		Control board when the switch is pressed. If absent, check continuity from pin 10 of IC J to pin 13 of IC A, pin 2 of IC Z, and pins 12 and 1 of IC P. Repair as necessary. Pins 2 and 14 of IC A should be HIGH. If not, trace continuity to Vcc. If the $\overline{DEP}$ pulse is still absent, check IC J according to the instructions on page 4-5. If IC J is working properly, and if continuity is present, check ICs A and H on the Interface board for proper logic operation.
F.	A HIGH S7 pulse should produce LOWs at IC F pins 1 and 15 and IC N pin 15 on the Interface board, and a HIGH at pin 6 of IC C on the CPU board.	If present, proceed to Step G.	If a HIGH DIGI pulse does not occur at bus pin 57, trace logic from IC C pin 5 on the Display/Control board to a LOW pulse at pins 6 and 12 of IC B on the Interface board. Trace the HIGH pulse from IC B pin 8 to a HIGH at pin 6 of IC C on the CPU board. Pin 2 of IC B should pulse HIGH simultaneously with IC C pin 6. If not, check the logic from pin 2 of IC B to pin 17 of IC M on the CPU board. Check the ICs, if necessary, according to the instructions on page 4-5. If absent, check for a CS signal at pin 4 of IC J and for HIGH pulses from IC P pin 12 to pin 5 of IC J on the Display/Control board. If the signals are absent, trace continuity and repair as necessary. Trace logic to IC B pin 12 on the Interface board. Pins 4, 5, 9, 10, 13 and 2 of IC B

Step	Instructions	If Correct	If Incorrect
			should be HIGH. If pins 4, 5, 9 or 10 are LOW, trace continuity to VR1 pin 2 on the Interface board. If pin 2 of IC B is LOW, trace logic and continuity to pin 17 of IC M. IC M pin 17 should be HIGH. If not, look for shorts and check IC V according to the instructions on page 4-5. If pin 13 of IC B is LOW, check IC J on the Interface board according to the instructions on page 4-5. Pins 12 and 13 of IC J should be LOW. If not, check ICs C and D on the Interface board according to the instructions on page 4-5. S7 should produce a LOW pulse at pin 12 of IC B, causing a HIGH pulse at pin 1 (of IC B). If a HIGH pulse is not present at pin 1, check IC B according to the instructions on page 4-5. Trace the HIGH pulse from IC B pin 1 to IC C pin 5 on the CPU board. (Pin 4 of IC C should be HIGH.) Absence of a LOW pulse at pin 6 of IC B will cause all "1's" to be deposited into memory (no matter how the AØ-A7 switches are set) when the DEPOSIT switch is pressed. Pressing the EXAMINE switch will cause HIGHs only at A3, A4 and A5 (no matter how the AØ-A15 switches are set), since the CPU receives an RST 7 (377) instruction and jumps to location 070.

Step	Instruction	If Correct	If Incorrect
	G. A HIGH S8 pulse should produce a HIGH READY pulse on pin 23 of IC M on the CPU board.	If present, proceed to Step 12.	If the READY pulse is absent at pin 23, check for a HIGH pulse (from IC P) at pin 1 of IC J on the Display/Control board and for a CS signal at pin 2 (of IC J). If the pulse is absent at pin 1, check continuity to pins 1 and 12 of IC P. Repair as necessary. If the CS signal is absent at pin 2, refer to Step 13 on page 4-23. Trace logic from pin 12 of IC J to a HIGH pulse on pin 11 of IC M1. Check any suspected ICs according to the instructions on page 4-5. Pins 12 and 10 of IC M1 should be HIGH. If not, trace continuity to Vcc. Pin 13 of IC M should be HIGH. If a constant LOW is present, check logic at ICs J1 and T1 and replace, if necessary. Trace logic from IC M1 pin 8 to IC M on the CPU board. Replace ICs and repair shorts or opens if necessary. If ICs M or F appear defective, refer to Section 4-3, Step 6 on page 4-20.
12	Check the DEPOSIT switch for proper operation; it should deposit each bit separately.	Proceed to Step 13.	If the switch cannot deposit the bits separately, try different bit combinations. A bit that cannot be deposited separately may be dependent on another bit; check for shorts with an ohmmeter set at X1K or higher. A LOW resistance reading between two data lines indicates a short. Repair as necessary.

Step	Instructions	If Correct	If Incorrect
13	Lower address switches A8-A15 in order to isolate any effect they may have on the circuitry. The switch symptoms should not change.	If there is no change in the symptoms, proceed to Step 14.	If the symptoms change when A8-A15 are lowered, check the logic operation of ICs W, U, Z, A1 and A. If necessary, check the ICs according to the instructions on page 4-5.
14	ICs B1 and T on the Display/ Control board are not needed for the EXAMINE, EXAMINE NEXT, DEPOSIT and DEPOSIT NEXT functions. If problems occur with these functions, turn power off and remove ICs B1 and T from the board. Removal of B1 and T will isolate any effects these ICs may cause. However, the switch symptoms should not change.	If the symptoms do not change, make sure power is off and reinstall ICs B1 and T. Proceed to Step 15.	If the symptoms change, check pins 1 and 2 of both ICs for LOWs. If absent, trace continuity to the Ground pin of the 7805 voltage regulator on the Display/Control board. Pin 13 of both ICs should be LOW. If not, trace continuity to pin 17 (for IC B1) or 15 (for IC T) of IC A. Repair as necessary. Pin 13 of both ICs should never pulse HIGH for the EXAMINE/EXAMINE NEXT or DEPOSIT/DEPOSIT NEXT functions. Pin 14 of both ICs should be HIGH. If not, trace continuity to Vcc (VR1 pin 2).
15	Examine the IC outputs in order to test the Display/ Control board's open collectors (ICs Y, W and U), the address switches and continuity to pull-up resistors R41-R48 by lifting up each address switch (A0-A15) separately.	Proceed to Step 16.	If any of the outputs fail to go HIGH when the corresponding address switch is lifted, check for a LOW input signal. If the input is not LOW, check for shorts and continuity to pin 21 of IC A. A LOW input signal indicates that a bad IC exists or that one of the components is holding the line LOW. Check Vcc and Ground to the IC. Pin 13 of both ICs B1 and T should be LOW. If not, trace continuity back to IC A and check IC

Step	Instructions	If Correct	If Incorrect
	A bad open collector can cause the switch data to be examined or deposited improperly. If an address switch is down, the corresponding open collector output is disconnected from Vcc and will float as a LOW. Lifting the address switch should raise the output of the open collector to approximately 4v. (Note: The common inputs of ICs Y, W and U should be LOW when the computer is stopped and no switches are pressed.)		A according to the instructions on page 4-5. Pins 1 and 15 of IC R and pin 1 of IC S (on the Display/Control board) should be HIGH. If not, trace logic to pin 10 of IC A. Test any suspected ICs according to the instructions on page 4-5. Check for shorts on both the Display/Control board and the Interface board along the FDIO-FDI7 lines.
16	A. If the ACCUMULATOR DISPLAY switch will not function, follow the steps below:		
	1) Check the ground strap from VR1 on the Display/Control board to the computer; it must be connected in order for the ACCUMULATOR DISPLAY switch to function properly.	Proceed to Step 2).	Repair as necessary.

Step	Instructions	If Correct	If Incorrect
2)	Make sure jumper JD to JC is present on the Interface board.	Proceed to Step 3).	Repair if necessary.
3)	Check for LOWs at pins 2 and 1 of ICs B1 and T on the Display/Control board. (A constant HIGH should be present at pin 14 of both ICs.)	Proceed to Step 4).	If pins 2 and 1 are HIGH, trace continuity to Ground (pin 3 of VR1) on the Display/Control board. If pin 14 is LOW, trace continuity to VR1, pin 2. Repair as necessary.
4)	As long as the ACCUMULATOR DISPLAY switch is held, pin 2 of IC G on the Interface board should be LOW. Pins 13 and 14 of IC G should be HIGH and pin 1 should be LOW.	Proceed to Step 5).	If pin 2 is HIGH, trace logic from IC G to IC Y1 on the Display/Control board. Check any suspected ICs according to the instructions on page 4-5. If pins 13 and 14 of IC G are LOW, trace continuity to VR1 pin 2 (on the Interface board) and repair as necessary.
5)	Pressing the ACCUMULATOR DISPLAY switch should produce LOW pulses at pins 8 and 9 of IC D on the Interface board. As a result, pin 10 of IC D should pulse HIGH. Pins 10 and 11 of IC K should also pulse HIGH.	Proceed to Step 8.	Since pulses are usually too rapid to detect visually, run the following program to generate several pulses.

Location	Bit Pattern
000	333
001	377
002	303
003	000
004	000

Step	Instructions	If Correct	If Incorrect
	If jumper JE to JF is present on the Interface board, a HIGH pulse should be present at pin 9 of IC K. The resulting LOW at pin 8 (of IC K) should produce a HIGH pulse at pin 11 of IC G.		(Note: Jumper JE to JF on the Display/Control board must be absent for the following check.) To check the levels of ICs D, J and G pin 4, stop the computer and examine to location 000. Lift the SINGLE STEP switch twice with the above program deposited into memory. If pin 10 of IC K is LOW, trace the SOUT logic to the CPU board. If pin 11 of IC K is LOW, trace the PWR signal to IC M on the CPU board. Check any suspected ICs according to the instructions on page 4-5.
B.	If the ACCUMULATOR DEPOSIT switch will not function, check the inputs of ICs B1 and T as described in Step 14 on page 4-65.		
C.	If the IN switch will not function, check the SENSE switch operation as shown in Table 4-9, starting on page 4-50.		
D.	If the OUT switch will not function, check the sense switch operation as shown in Table 4-9, starting on page 4-50.		